Proposal for the TPC Electronics and Data Acquisition Upgrade for STAR

"DAQ1000"

March 22, 2005

The STAR DAQ1000 Group

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Executive Summary

The STAR Collaboration proposes to replace the Time Projection Chamber (TPC) detector readout and Data Acquisition (DAQ) electronics. The new frontend electronics will be based on two CERN/ALICE developed custom ASIC chips, the "Preamplifier/Shaper" (*PASA*) and the "ALICE TPC Readout Chip" (*ALTRO*.). Events will be transferred to the TPC DAQ system using a CERN/ALICE developed fiber optic link, the "Detector Data Link" (*DDL*). The TPC DAQ backbone will be built using off-the-shelf commodity PCs interconnected with standard gigabit network links used for data movement. This project has been dubbed *"DAQ1000"* due to its expected event rate capability of about 1 kHz.

This upgrade will significantly improve STAR's data taking capabilities and will be beneficial to all of STAR's current and foreseen physics programs. The expected event rate of more than 1 kHz (as opposed to the current hard limit of <100 Hz), the exceptionally low associated deadtime (less than 100 μs compared to the current 10 ms per event) and the physical redesign of the TPC Readout Board electronics (creating 4 inches of additional space) will:

- increase STAR's data taking rate more than 20 times for minimum bias Au+Au collisions. It will increase the data taking rate by up to 50 times in other collision systems (or energies) where the number of measured tracks in the TPC is smaller. This will offer increased benefits when studying systems such as polarized protons and lighter nuclei as well as during lower energy runs.

- increase the data taking rate of rare triggers by a factor of two across the whole physics program. This would be effectively equivalent to a factor of two increase of RHIC's average luminosity.

- allow newe detectors to be installed in the space between the TPC endcaps and the Endcap Electromagnetic Calorimeter. Due to the smaller size of the new TPC electronics boards STAR can install new tracking detectors in this region which are essential for STAR's W program in polarized pp collisions.

This rate increase is well matched with STAR's current fast detectors (i.e. both electromagnetic calorimeters whose rates currently exceed 3 kHz) and all of the proposed STAR upgrades programs (most notably the new Time-Of-Flight (TOF) detector) whose designs already incorporate data acquisition electronics capable of sustaining rates beyond 1 kHz at low deadtime.

The development of this new DAQ system is made possible by the availability of custom electronics ASICs designed for the CERN/ALICE TPC. The ALICE collaboration has demonstrated reliable performance using these custom ASICs and has already completed their full chip order, as well as testing, and is currently undergoing full installation. The fiber-optical components of the DAQ chain (so called *DDL* links) were also fully designed and debugged at CERN and in addition are currently in use for physics

production in STAR's TOF prototype. These optical links are envisioned to be used in all future STAR detectors as the DAQ detector links.

R&D for this upgrade program has already started and is currently in the prototyping phase made possible by the RHIC R&D funds. The first prototypes are expected mid-2005 (during FY05) while the final electronics construction is proposed to begin at the start of FY07 and be ready for a presumed RHIC run in FY08.

The total cost of this project is estimated to be $1.8M where a major item ($500k) is for Non Recurring Engineering (NRE) costs incurred by CERN for certain aspects associated with the intellectual property of the developed ASIC chips. Additionally, due to the manufacturing contract expiration in June 2005 the whole ASIC electronics complement must be ordered before this date. This represents about $350k and is a crucial step for this project.

Physics Goals

By the nature of a data acquisition system and the central role the TPC plays throughout STAR's physics programs all of STAR's physics goals benefit significantly from this upgrade.

Soft Physics

In the so-called soft physics (non triggerable, i.e. minimum bias) data sets the obvious benefit is the increase of the data taking rate by a factor of 10 or more. This not only means that STAR can take more data (events) in the same amount of RHIC running time but also that STAR will have the option of running a shorter time at a given energy or species while maintaining the same event statistics. This is certainly beneficial for any kind of energy or species scanning in heavy ion collisions (such as the current copper run at 3 different energies) where STAR can take ample data in very short amounts of time at a given species/energy set point. The increase in rate might also be beneficial in the case of shortened RHIC runs due to financial budget constraints, in that the physics program of STAR will not be affected as much.

Some of the more challenging measurements require the acquisition of very large data sets for precision and rare process studies such as:

- b-quark jet quenching
- CP violation search
- Gamma-gamma HBT

Rare Physics

In the so-called rare physics (triggerable) data sets the major benefit of this project is the decrease in the TPC/DAQ deadtime while at the same time maintaining the high rate for soft physics. Due to the current TPC/DAQ constraints, STAR is running typically at a 50 Hz rate at 50% associated deadtime. The 50 Hz of events also typically contain about 20-30 Hz of soft physics events (minimum bias) while the other 20 Hz are reserved for the rarer triggers (such as high P_t particles, jets, forward π^0, upsilon, J/Ψ etc.). In the proposed new modes STAR would essentially run deadtimeless thus harvesting *two times more* rare probes while at the *same time* acquiring the soft physics data.

An additional benefit of this upgrade is to the Ultra Peripheral Collision (UPC) program where the event size is negligible and in principle incurs no penalty such as event storage, deadtime or even offline analysis resources. This is currently not the case since the current TPC electronics exerts the same deadtime penalty of 10ms/event *regardless* of charge occupancy making the UPC program severely constrained. With the new system, however, the resources used are proportional to the event size.

Forward Rapidity Physics at 500 GeV/c Proton Collisions

A major future program in STAR's spin physics is the measurement of the spin asymmetry in the decay of W bosons which will enable us to map the contributions of sea antiquarks of different flavor to the spin of the proton. This proposed program will be carried out by measurements of the high energy decay daughters of the W in the STAR Endcap Electromagnetic Calorimeter (EEMC).

The momentum of electrons from the decay of the W is expected to be 20 GeV/c or above which, coupled with their detection in the forward rapidity region by the EEMC, makes the TPC inefficient as the tracking detector. Since the crucial element is the determination of the charge sign of the decay daughters, STAR has proposed to install a new tracking detector in the forward rapidity region between the TPC endcaps and the EEMC. However, such an upgrade is presently physically not possible due to the large size of the current TPC electronics RDOs. This upgrade project would easily solve this issue by making the new TPC electronics about 4 inches shorter due to the more modern/dense electronics available today.

Design

Introduction

The DAQ1000 Project consists of the following components:

TPC frontend electronics (FEE) cards, TPC Readout Boards electronics (RDO), the fiber link towards the DAQ system (DDL), DAQ Receiver Boards (RORC), DAQ-TPC Sector CPUs, DAQ backbone interconnect and finally the DAQ Event Builders (EVBs).

Many these components are off-the-shelf commodity items and do not need any hardware development (such as Sector CPUs and Event Builders), some of them will be purchased as already made custom boards from a CERN-related manufacturer (such as the DDL optical link and DAQ Receiver Boards) while two components need to be designed, manufactured and installed by the DAQ1000 Project Group: the TPC FEE eand the TPC RDO electronics boards.

TPC Front End Electronics Cards (FEE)

The new TPC FEEs are proposed to be direct replacements for the current electronics cards. They will be exactly the same size and they will connect in exactly the same manner to the TPC padplane. This has been done so that no changes are necessary to the TPC padplane.

The new FEEs will each be capable of handling 32 channels of electronics (same as now) by housing 2 preamplifier/shaper custom ASICs (CERN/ALICE/TPC *PASA*) and 2 ADC/filter/storage custom ASICs (CERN/ALICE *ALTRO*).

The PASA is a 16 channel analog preamplifier and shaper which amplifies the raw electronics signals obtained by charge induction at the TPC pads in a manner similar to the current STAR TPC as well as the ALICE TPC.

The amplified, differential outputs of the PASA are fed into the ALTRO chip where they are digitized, digitally filtered and additionally shaped, pedestal subtracted, zero-suppressed and finally buffered on chip awaiting subsequent readout. The ALTRO chip is the heart of the proposed upgrade and its availability is a crucial part of the project. The sophistication of this ASIC, as well as its reasonably low cost, makes the whole project feasible in the envisioned time frame and budget.

Finally, the digitized and stored data are translated from a TTL signaling standard (suitable for short distances) to a GTL+ standard (suitable for distances of up to 1 m) and onto a 68-pin flat ribbon cable and into the TPC Readout Board for further storage and shipment to DAQ. The ALTRO chip itself can buffer up to 4 whole TPC events which makes the derandomization very convenient.

The ADC stage of the ALTRO can be clocked synchronously at up to 20 MHz. Although we plan to synchronize it to the RHIC clock (about 10 MHz) similar to the current STAR TPC it is worth noting that we could attempt to run it at a higher clock speed in case STAR wishes to run the TPC at a faster drift velocity (i.e. by changing the gas mixture and/or increasing the drift field). The faster drift would allow the TPC to have less pileup due to potentially higher RHIC luminosities at later years.

The digital readout clock is a completely separate clock from the digitization clock and can be any value up to 40 MHz. At this R&D stage we are assuming that we will use a value between 20-30 MHz depending on other components in the system. The ALTRO readout bus is a 40 bit wide bus and running it at the maximum rate of 40 MHz one can obtain a throughput close to 200 MB/s/FEE which is far above the necessary rate.

This new FEE is a pipelined system with the real-time digitization of the triggered event running fully in parallel with the readout of the previous event(s). This enables the fixed deadtime of the system to only dependen on the intrinsic TPC drift velocity (currently about 40 μs for one event). As the zero-suppression is performed on the ALTRO before it is buffered the other, readout related, sources of deadtime will depend strongly on the amount of charge (or tracks) in a particular event which is unlike the current TPC where any event takes 10 ms to read out regardless of occupancy. Preliminary results show that this readout related deadtime can be absorbed for charge amounts ("event sizes") equivalent to minimum bias Au+Au collisions at rates of up to 1 kHz and for smaller event sizes at rates of up to 5 kHz.

The sensitive grounding issues related to the connection of the FEE to the TPC padplane are believed to be well understood already in the current TPC electronics and this successful design has been copied over to the new FEE. Additional care was taken to separate the analog grounds (PASA & padplane) from the digital grounds in a manner similar to the current (working and tested) CERN designs.

The new FEE is expected to need only about ½ the power of the current TPC FEE as an additional benefit. Nevertheless, the new FEEs will have the same excellent cooling brackets as the old STAR FEEs which we plan to reuse in the new design.

The FEE prototype work is in progress (funded by RHIC R&D funds) and is in the final layout phases at the time of this writing (March 2005). Due to a relatively simple electronics design, CERN's and STAR's experience with their respective TPC's and associated electronics we assume that this card will need only one prototyping stage and have already designed it as a fully functional final version.

The layout of the new FEE card is shown in Figure 1 (top side) below.

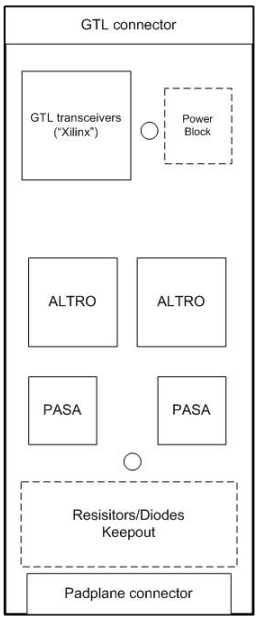

Figure 1: The new TPC FEE Block Diagram

TPC Readout Board (RDO)

The RDO is the custom electronics board which gathers the digitized data from a number of TPC FEEs, buffers it and finally transmits the data via optical links off the detector to the DAQ Room of the STAR experiment.

The organization of new RDOs follows the same scheme as the current RDOs: there are 6 RDO boards per TPC sector totaling 144 RDOs for the whole TPC. Whereas the current RDOs are actually connected pairs of 1 master RDO and 0 or 1 slave RDOs (depending on the radial location at the padplane) the new RDO will be a much simpler single board. Additionally, due to the requirement for a new tracking detector at the ends of the TPC, the new RDO will be about 4 inches shorter to accommodate additional detectors in this space.

The new RDOs are conceptually similar to the old RDOs and they will be located at the exact same positions as the old RDOs. This means that the current mounting and cooling aluminum brackets will remain intact and the new boards will maintain the same mounting holes and systems as the old ones. The new RDOs will thus easily replace the old ones without any other special tools making the installation very easy.

The RDO is essentially a large multiplexer which reads out the data from multiple FEEs (up to 36 per RDO, depending on the radial position of the board) and channels it onto a single optical fiber. The new board will maintain the same topology as the old one except that the ribbon cable and the connectors from the FEE will be replaced by a higher density technology (a SCSI-3 standard cabling) due to the 40 bit bus between the new FEE and the new RDO.

The new RDO connects to the STAR Trigger Interface in exactly the same manner as it does now (20 pin connector using PECL signaling) thus keeping the same cables and interconnect styles to the Trigger.

We are proposing to replace the current powering scheme with a new one although we shall keep the same power cables and connectors and reuse them for the new board. Since we wish to maintain the low power consumption of the new electronics (1/2 the current one) as well as to maintain a better electrical ground separation between the analog and digital sections of the FEE (which gets its power via the RDO) we propose to replace the current +8V and -8V power supplies with two +5V power supplies each with separate grounds. This will add only a modest cost increase but will significantly decrease the dissipated power since the new electronics will use only +3.3V (or lower) voltages. The decoupled grounds will also decrease the potential for noise coupling via the grounding lanes.

Each RDO houses an optical-fiber daughtercard developed and manufactured by CERNtech, Hungary, for the CERN/ALICE data acquisition system. The daughtercard is dubbed *Source Interface Unit* (SIU), while the optical link protocol as well as the whole network is termed the *Detector Data Link* (DDL). This card (Figure 2) is readily available through the manufacturer and is currently in use in the STAR TOF prototype with excellent results. The commercial availability of this module significantly shortens our R&D phase. The DDL is a bidirectional point-to-point network with a demonstrated maximal throughput of 200 MB/s. We have been using these cards in test setups within our DAQ1000 project in the past year with excellent results.

The bidirectional nature of the link is a requirement since the ALTRO performs zero-suppression and pedestal subtraction on chip thus necessitating the pedestal tables and other configuration parameters to be loaded from the DAQ system back to the TPC frontend. As an additional bonus the new RDO will not have a separate slow controls interface as all the necessary control can be obtained using the same optical link as the data.

The new RDO is currently in the prototyping stage supported by the RHIC R&D funds. A prototype card is expected around June 2005 which fits with the availability of the prototype FEE. However, since the RDO is a relatively complicated device we decided that we will first produce a simple, conceptual prototype which will be only able to read 4-6 FEEs at the same time instead of the full 36. This prototype will enable us to get experience will all of the facets of the board but will not burden us with the routing and complications of additional connectors.

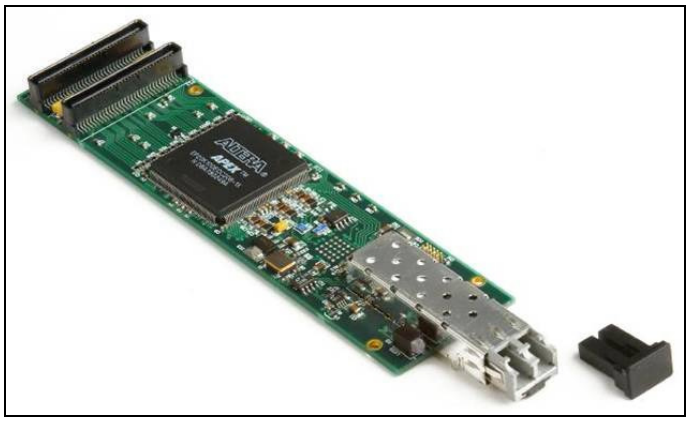

Figure 2: CERN/ALICE SIU optical daughtercard

TPC Receiver Boards (D-RORC)

The board which receives the digitized TPC data is developed and manufactured by the same company (CERNtech, Hungary) which developed the TPC sender daughtercard (SIU) and is the other part of the optical link. The name of this board is *D-RORC* and is commercially available from the developer, same as the SIU. A D-RORC board is shown below.

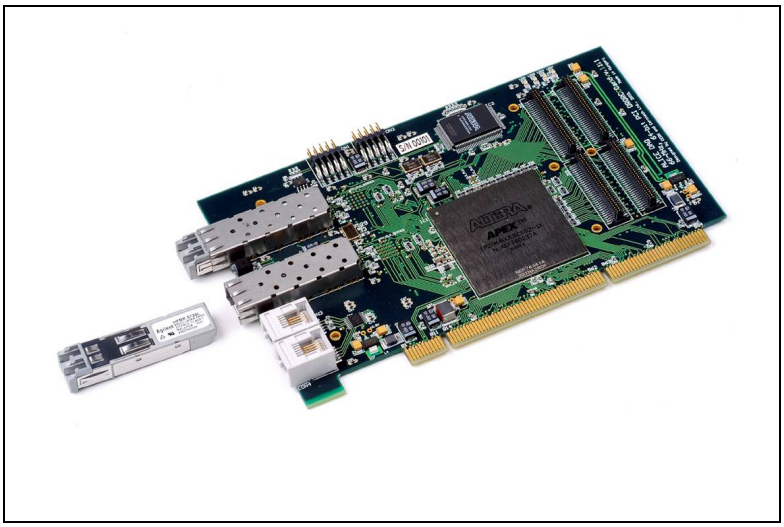

Figure 3: CERN/ALICE D-RORC Optical Receiver PCI Board

It is a PCI64 standard, 66 MHz, 3.3V compliant PCI card which can be plugged in any compatible PCI slot of a host computer (PC). The D-RORC houses two independent bidirectional DDL links on the same card sharing the same PCI bus host interface. The firmware of the card is designed such that it uses the host computer's DRAM as the buffer memory thus providing very low latency transfers without any host intervention (apart from the buffer setup which is typically done only once at startup).

We have significant experience with this board both in DAQ1000 tests and in real physics production with the TOF detector prototype. The board and the Linux-based host PC can demonstrably sustain 200 MB/s per fiber and software is already written to support its features.

The dual fiber nature of this board cuts the quantity of these boards by half and we plan to install 3 of these boards per PC computer totaling 6 DDL links. In this natural topology we would assign one PC to one specific TPC sector.

TPC Host Computers

The computers which host the D-RORC cards are called the Sector Computers since they will receive data from one whole TPC sector over 6 DDL links, 2 links per card for a total of 3 D-RORC cards per computer, at least in the first instance of this project.

They are assumed to be rack mountable dual CPU PCs outfitted with the fastest CPUs available. The operating system of choice is a freely available Linux variant. Apart from hosting the D-RORC cards the main purpose of these CPUs (and the reason for their large processing speed requirement) is running the cluster finding algorithm. It has been already demonstrated in the FY04 (Au+Au, p+p) and FY05 (Cu+Cu) RHIC physics runs that the STAR TPC *Fast Clusterfinder* (FCF) is a powerful algorithm which can process the raw TPC ADC data in real-time and extract the two-dimensional coordinates and the deposited charge of particle tracks traversing a TPC padrow. Apart from the demonstrated data compression of more than 5, this way of operating has the significant added benefit of offloading the Offline software from this very time consuming processing stage. In the two most recent RHIC runs (FY04 & FY05), STAR has exclusively relied on this mode of running, enabling STAR to gather data almost 10 times faster than design. This mode of operation (called *"DAQ100"* due to the 100 Hz of event rates it makes possible) is the main reason for the large data samples that STAR has taken in the last 2 years of RHIC running.

In the first instance of this project we plan to connect 3 D-RORC cards (one whole TPC sector) to a single dual-CPU computer. Later, if resources become available and there is physics interest we can trivially scale the processing power by adding more computers and associating i.e. only one D-RORC per machine for a factor of 3 increase in speed.

These machines will contain two gigabit Ethernet links to the STAR DAQ Event Builders to which the data output of the cluster finder will be sent. The gigabit links present no additional cost since every modern PC computer already contains them mounted on the motherboard.

DAQ Network & Event Builders

The DAQ backbone network is proposed to be gigabit Ethernet which has become a very low cost network in the last years. This represents a departure from our current Myrinet

network which will make the whole DAQ system cheaper and easier to maintain while still keeping the high data rates required.

We do not propose to change the current DAQ event builder machines at this stage since the four that we have can keep up with the envisioned rates with modest upgrades obtained via standard operations funds. The event builder scheme which we already have in place is well suited to the proposed upgrade and is easily scalable in the future if needs arise.

DAQ Modes of Operation

In the DAQ1000 era some of current STAR's detectors will not be able to keep up with the high rate available after the TPC & DAQ have been upgraded and will remain "slow" detectors.

These detectors are the Silicon Vertex Tracker (SVT), Forward Time Projection Chambers (FTPC), Photon Multiplicity Detector (PMD) and possibly the Silicon Strip Detector (SSD). The SSD might be capable of sustaining these rates after modifications of its readout electronics but this is still uncertain at this time. All of the other detectors (Barrel & Endcap Calorimeters, the new Time-Of-Fight (TOF)) as well as all of the new proposed detectors (i.e. the Forward Meson Spectrometer (FMS), the misc. forward tracking detectors etc) will be able to sustain rates in excess of 1 kHz and are thus compatible with the DAQ1000 upgrade.

The DAQ & electronics of all these older slow detectors will be maintained as-is thus STAR DAQ will operate in split-detector mode – only detectors which are "live" at any moment will be read out in a specific event. This will create two possible mixtures of detectors for any given physics trigger: *fast only*, when any of the slow detectors is busy processing a previous event, and *fast+slow* when all of the detectors are alive (the typical current STAR mode of DAQ readout). The effect of this operation will be that the slow detectors may only be available in 10% of the events (depending on physics rates and general STAR needs) but causing no other issues to be dealt with. In other words, the slow detectors will be present in exactly the same number of events that they would be regardless of the DAQ1000 upgrade.

Construction and Installation Schedule

The construction and installation is proposed to occur in 3 major stages (milestones) which are matched to the current and upcoming fiscal years FY05-FY07:

1. The design, construction & testing of the FEE & RDO prototypes.
2. Design and construction of the final FEE & RDO and their installation in one whole TPC Sector
3. Final construction and installation of the full electronics in the remaining 23 TPC sectors.

Stage 1: Prototypes (FY05)

The prototyping stage is currently an ongoing effort funded through RHIC R&D support. The deliverables of this stage are a fully working FEE prototype and a fully working (but not fully sized) RDO prototype. The prototype FEE is assumed to be very close to the final version and the main purpose of the prototype is verification of the functionality of the CERN ASICs as well to gain experience in handling and programming the complicated ALTRO chip. The RDO prototype will also be a fully functioning RDO except that the number of channels/FEEs that it will be able to handle will be only 1/4 of the total.

Both of these 2 crucial prototypes will be installed in the TPC in a parasitic mode with a parasitic DAQ and will be used to verify the whole design while STAR is actually taking physics data early in FY06 (i.e. November 2005). In case the FY06 RHIC run is postponed we would attempt a full test with cosmic rays either using the current TPC or using a test sector in the lab. This has not yet been determined.

In parallel to these tests and debugging we would continue designing and developing the full RDO prototype with the expectation of having a final prototype in hand by late 2005 or early 2006.

During this fiscal year (FY05) we must obtain the full contingent of the CERN chips, both ALTRO & PASA since the ALTRO contract expires in June 2005 and the PASA shortly after.

Stage 2: Single sector readout (FY06)

When the final designs of both the FEE and RDO have been developed we plan to construct and install a whole new TPC & DAQ system in one sector of the TPC only. This crucial step will allow us to run the newly upgraded system in all the ways we envision.

This stage will enable full online debugging and final cross checks of the new electronics while posing only a small risk to the overall TPC physics running. One sector is only 1/24 of the whole TPC.

The goal of the second stage is to be ready for the RHIC physics run in FY07 (i.e. November, 2006). At this time we also expect a similarly sized TOF prototype and we would match its coverage to effectively create a single-armed spectrometer running at high rates (1 kHz or more) in parallel to the rest of the STAR TPC. If there is sufficient physics interest and resources we might attempt to equip 2 TPC sectors in a back-to-back topology and try to measure two particle decays with this device as well. This has not yet been decided.

Stage 3: Final construction & installation (FY07)

The final construction followed by installation is proposed to proceed throughout FY07 to be ready for the FY08 RHIC physics run assumed to start in Q4 calendar 2007.

The details of the construction of the FEE & RDO cards have not been finalized yet but it is assumed that a non-BNL facility will be involved with the production, testing and partly with the final installation of all of the custom electronics. At the time of this proposal such facility is assumed to be the Bates Laboratory at MIT but no formal arrangements have yet been proposed. Final details of this involvement will be finalized throughout FY05/FY06.

The installation will have to wait until the end of that year's RHIC physics run after which the deinstallation of the current TPC electronics will commence. The current RDOs will first be removed followed by all the current FEEs. The cooling brackets of the old FEEs will be removed and mounted on the new FEEs after which the new FEEs will be installed onto the TPC padplane followed by the installation of the new RDOs. As soon as i.e. one sector of the TPC has been installed the verification can proceed in parallel with the installation of another sector.

The following table shows graphically the proposed timeline and schedule with the 3 major milestones shown in bold font. Years shown are calendar years.

		05				**06**				**07**		
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Prototypes												
RDO proto												
Proto. Tests (1)												
Sector production												
Sector installation												
Sector test & run (2)												
Full production												
Installation												
First physics (3)												

Table 1: Project schedule and timeline

The installation of both the single sector and the full electronics is strongly predicated on the RHIC running schedule and must be adapted to match. Obviously, installation cannot proceed during the RHIC running periods and, conversely, many tests can not be done if RHIC is not running.

Preliminary Cost Estimate

The total cost of the project is estimated at $1.86M which does not include any overhead but does include 20-25% of electronics spares. Apart from the procurement of the essential electronics from CERN, the 2005 fiscal year is proposed to be funded from the RHIC R&D sources as well as small part of FY06. None of these costs is shown in the table. The manpower is assumed to be contributed by the institutions which are part of the project both for engineering as well as production support, Q&A and installation. Note that the CERN electronics contributes almost ¾ of the total cost and is thus very sensitive to the dollar vs. euro exchange rates. The exchange rate in this estimate is assumed to be 1.34 $ = 1 €. Another large item worth noting is CERN's NRE cost of the ALTRO chip which covers part of CERN's expenditure for a) intellectual property paid to the ALTRO manufacturer (ST Microelectronics) and b) mask setup paid to the ALTRO & PASA manufacturers for the chip fabrication.

Item	Description	Cost (k$)	Comment
FEE			
(5200 boards)	ALTRO	731	435 k$ are CERN NRE, 67k$ testing
	PASA	162	42 k$ are CERN NRE, 15 k$ testing
	Other components	276	Includes PCB production and stuffing
	Total	1169	
RDO			
(170 boards)	SIU	142	
	Other components	229	Includes PCB and stuffing
	Total	371	
DAQ			
	D-RORC	191	
	Fiber	29	30 km of optical fiber…
	PCs	104	
	Total	324	
Project Total		**1864**	

Table 2: Project Cost Estimate.

Finally, this estimate will remain preliminary until the prototypes have been fabricated and verified at which point a real cost of the project can be established.

The following table shows the proposed distribution of resources by fiscal year. The additional ASIC testing is a chip-by-chip test at Lund, Sweden for both ALTRO & PASA and could potentially be somewhat lower than the $80k indicated. However it is important that it be done before the ASICs are actually used in FEEs.

Item	FY05	FY06	FY07
ASICs manufacturing	330		
CERN NRE		487	
ASIC testing		80	
Single sector electronics		32	
D-RORCs		191	
SIU cards		142	
Complete electronics			470
DAQ Computers, fibers			132
FY totals	**330**	**932**	**602**

Table 3: Proposed cost distribution along fiscal years

The D-RORCs and SIUs should be also purchased at an earlier time due to the assumed matching dates for ALICE production. Best would be if they are procured already in FY06. However they can probably be moved into FY07 if necessary.

DAQ computers and fibers should be purchased at the latest date possible taking advantage of Moore's law and could possible be moved into FY08, depending on the RHIC physics running schedule of those fiscal years.