The STAR iTPC Upgrade Robert Pak for STAR Collaboration





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STAR: Solenoidal Tracker at RHIC iTPC: inner Time Projection Chamber



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Expanding the coverage to y = 0.8 increases the significance by a factor of 3. Low energy cooling from LEReC reduces uncertainty due to higher luminosity.



close-up cross section

anode wires spaced 4 mm apart, ground shield and gated grids spaced 1 mm apart



- 40 pad rows fit perfectly with existing grid
 - identical pad response function on both ends of the grid
 - no need to change the grid; wire locations remain the same
 - no need to add more wire mount channels

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new iTPC pad plane

- increase coverage with higher density front end electronics
- relatively large area printed circuit board was challenging
 - minimize trace lengths to reduce capacitive noise
 - same number of connectors as original inner sectors
 - same number of even/odd pads per connector for backward compatibility
 - same mounting brackets and cooling manifolds





pads on the front Robert Pak (BNL) 5

pad plane connector layout on the back



- aluminum support frame for iTPC sector
- original drawings (circa 1993) used to create 3D CAD model
- slight modifications:
 - slots for iFEE cards moved by 5.6 mm
 - walls to mitigate grid leak added





strongbacks fabricated at IMT Precision in Hayward, CA



MWPC assembly process

- @ LBNL:
 - bond pad plane to strongback
 - machine O-ring groove
 - prefit wire mounts
- In China SDU, USTC, SINAP



- wire grid plane production started Feb 2017
- -1^{st} production version arrived at BNL in Sept 2017
- sector tests (HV burn-in, gain uniformity and stability)
- 24 sectors + spares delivered (last shipment Oct 2018)
- @ BNL:
 - testing of all fully assembled modules before installation



facilities at Shandong University



wire pitch and tension controlled by wire winding machine

clean room with granite tables for assembly

not shown: wire tension measurement system and cosmic ray test stand

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mounting of wire grid planes

anode, ground shield and gated grid planes mounted at SDU

Wire	Diam. (µm)	Pitch (mm)	Composition	Tension (N)
Anodes	20	4	Au-plated W	0.50
Anodes— last wire	125	4	Au-plated Be-Cu	0.50
Ground	75	1	Au-plated Be-Cu	1.20
Gating grid	75	1	Au-plated Be-Cu	1.20



combs for final wire alignment

10 micron tolerance achieved on wire pitch and height above pad plane

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designed by STAR Electronics Group





DAQ Receiver





electronics



- iFEE based on current FEE layout, but using SAMPA ASIC
- twice the number of channels per FEE as compared to previous FEE



test bench set up at BNL

prototype iFEE card sans SAMPAs

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installation tool and platform

designed by STAR Technical Support Group





 machined at UIC and BNL shops

<image>

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installation of iTPC sectors



all 24 iTPC sectors have been successfully installed

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The iTPC upgrade:

- 1) extends the accessible rapidity range
- 2) reduces the low p_T cut-in threshold
- 3) improves dE/dx resolution

During the 2018 RHIC run an iTPC sector was installed at the 8 o'clock location (sector 20) on the east side of STAR detector.

results from the 2018 RHIC run

The iTPC upgrade improves the dE/dx resolution:

simulation

Summarizing:

- Successful engineering run for iTPC project in the 2018 RHIC run
- All 24 iTPC sectors have now been successfully installed, electronics are next
- Stay tuned for results from the beam energy scan starting Feb 2019