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A Possible Level 0 Trigger Scheme for the STAR EMC[1]

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OUTLINE:

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Abstract

We propose a level 0 trigger for the STAR Electromagnetic Calorimeter, EMC, which provides a global energy sum and sums over cells appropriate for triggering on direct gammas and jets. It is implemented in analog at low level and digitally with FPGA's at higher level. I will provide trigger information in less than 800 nanoseconds.

1 Why Analog in the EMC Trigger?

We need a very large reduction in trigger rate at level 0. The interaction rate (min. bias trigger rate) can be one interaction per 110 ns bunch crossing time, or about 10^7/sec. The TPC readout may be only 100/sec. There is then a factor of 10^5 reduction needed to find the useful events.

Typical collider detectors have:

- single tower E_t
- cluster E_t
- global E_t

Since we don't have a Hadron Calorimeter, we need to do even better with the EMC. In order to trigger on Jets, gammas, and electrons, we want all possible :

- 1 tower sums
- 4 tower sums
- 9 (or 16) tower sums

including all overlaps within a very tight time budget before the TPC gate. The time includes all cable delays, integration times, and settling times in addition to processing. There will be 1140 of the 4 tower sums and 1080 of the 9 tower sums for a 1200 tower Barrel calorimeter, and more with the End Caps. Several people have told me that this cannot be done digitally without massive duplication. While a global sum could be done digitally, duplicating the first few layers of a PLA adder tree 1000 times becomes prohibitive. As an example, 53 Programmable Gate Array chips at $ 250.00 each might be needed for a global sum utilizing the digitized outputs from the analog parts of the trigger, but roughly 3000 chips would be needed to do everything digitally.

Another consideration is the ease of upgrading eg. the Barrel from 600 or 1200 towers to 4800 phototubes if both depth segmentation and finer eta segmentation is needed. Local analog sums would naturally accommodate this into the trigger since these would most likely be lumped together at level 0 and used separately only at level 3 trigger.

2 Trigger Requirements

We would like to satisfy a number of difficult requirements in the Level 0 trigger:

1. We want to do both QGP Heavy ion physics and high P_t AA and PP physics with as much in common as possible. (There are questions about what must be done simultaneously, however)

2. In a high luminosity situation, we may want as much as a factor of 10^5 reduction in trigger rate. We may need to go from 2×10^7 interactions per sec to 2×10^2 or 1×10^3 TPC reads per second. (The beam crossing rate is 9×10^6 per sec and there may be more than one interaction per crossing.)

3. The trigger should not have any dead time for beam crossings 110 ns apart. (Actually, we might build a first generation system for a 220 ns crossing time and upgrade it later.)

4. The trigger will have to provide a result in to 800 ns, from beam crossing to output of the cable at the TPC gate. This is needed to provide a gate for the TPC readout and SVT readout. The TPC HV on the gating grid must be changed and SCA clocking started. Data that drifts during the trigger processing time is lost. Cable delays may use 300 ns leaving little time for other delays in the trigger.

5. We want single tower, 4 tower and 9 tower (or possibly a form of 16 tower) sums with no boundary effects. This is for Jet, direct γ, electron and π^0 triggers.

6. We want a global E_t trigger which will add up very small (10 MeV to 500 MeV) signals from several thousand photo tubes to a total of 1 TeV or so. We assume this can be done by using the amplified one of two levels of analog signals, either integrated or shaped, from each photo tube. For example, there might be x 1 gain and x 32 gain signals. This also implies no zero suppression in the readout.

7. We want about 3 simultaneous programmable trigger levels for the 1, 4 and 9 (or 16) tower sums with the x 1 signals. For example, at 3, 9 and 20 GeV.

3 Other Readout Method Considerations

It has been suggested that in order to minimize the readout data bandwidth, a local threshold be used at each phototube, and that the phototube not be digitized unless the integrated level surpass a threshold. A simple example of the bias produced in comparing pp to Au Au with such a method is presented, and it is suggested that this be studied further with a simple model of the P_t distributions.

First, some simplified assumptions about the physics:

For PP there may typically be 6 charged pions in the barrel and 3 π^0 with the two γ's from each in the same or nearby towers. For AuAu there may be 2000 charged tracks and 2000 γ's so there could be three hits in each of the 1200 towers. The energy per tower has a varying relationship to the p_t spectrum as a function of A.

PP	typical	9 towers hit	$< p_t >\sim 0.3$ GeV/c
AuAu	typical	all 1200 towers hit	$< p_t >\sim 0.15 - 0.3$ GeV/c

Next, the missed energy with various thresholds for the PP vs AuAu:

	PP	AuAu
Tower Threshold	avg. error	avg. error
0.05 GeV	16%	13% – 7%
0.1 GeV	33%	26% – 13%

This should really be studied with P_t distributions to find both the number of towers missed and the more accurate measure of the energy missed.

I have done measurements of the noise level from a phototube plus an amplifier with x 100 gain. The rms noise level was about .003 Gev equivalent, assuming 1.5 pe per mip per layer in scintillator and 21 layers of scintillator in the calorimeter. We would want to be at least 4 or 5 σ above this if the digitization rate were to be reduced enough to justify this method. The coherent noise level from pickup is unknown.

4 Trigger Proposal

My proposal is to do local summing by analog means near the towers involved, and do global summing digitally using the outputs of the 9 (or 16) tower analog sums. The reason for this is that it is the only way I have found to do the 4 tower and 9 tower sums fast enough (300 ns) without boundary effects (taking all possible clusters) and without duplicating a digital FPGA layer a few thousand times. The analog signals are somewhat localized, a radius of 6 feet or so. The digital signals traverse the size of the STAR magnet. All this could be done with both the x 1 and x 32 signals in parallel. There is some possibility of using one level at a time with analog switching which would save a lot of money but the physics needs have not been completely analyzed for this. See Fig. 1–4.

As an example, if we have about 1000 towers in the calorimeter we can make single tower, 4 tower and 9 tower sums and their triggers locally (within a few feet) near the 1, 4 or 9 towers involved. If we have all possible 9 tower sums, we can take the subset of these that do not overlap, about 133 to 160 sums for the barrel, and digitize these locally. The digital information can be summed in tree fashion with FPGA's with a fast clock. This involves a tree of depth 8 or 9 instead of the 10 or 11 that would be required if all sums were digital.

A variation of the overall scheme is to do 1 tower and 4 tower sums and do 4-group sums of the 4 tower sums, instead of the 9 tower sums. The 4-group sums would take all the overlapping 4 tower sums and would cover patches of 16 towers with effective tower sizes of 4 towers. This may be at least as good for triggering on jets as the 9 tower sums. Only 270 of the 4-group sums would take care of all overlapping combinations on the Barrel, and there are only 75 non-overlapping sums for the global E_t. A detailed Monte-Carlo comparison is needed.

THINGS TO BE STUDIED: (some of these are analyzed later in this paper)

- Can we do a tree sum 8 or 9 layers deep in less than 300 ns total delay and with a new input every 110 ns? (probably yes)
- We have integrators or shapers at gain 1 and gain 32 on each tube (or tube card) with a fanout of 15 from each one? (probably differential twisted pairs with shield?) The fanout is used as follows: 9 for the 9 tower sums, 4 for the 4 tower sums, 1 for the 1 tower sum, 1 for digitization for readout and 1 for looking at analog signals with a scope through a cable.
- Can we have 1000 summers with
  - 9 inputs and 4 outputs
  - 4 inputs and 4 outputs, and
  - 1 input and 4 outputs

  spread in a web over the outside of the experiment with low noise? Can this be done with differential instrumentation amp style inputs (video amps)? Can this be done for both the x 1 signals and the x 32 signals? Should this be done simultaneously for the x 1 and x 32 signals?
- We have 3000 comparators, 3 per sum? This is to do the triggers at 3 levels for each of 1 tower, 4 tower and 9 tower sums using the x 1 signals.
- Do there exist chips to do these sums with differential inputs and outputs?
- How much of this could be put on an ASIC? (do we want to?)
- Is there any point in doing more summing by analog methods rather than digital after we have achieved our primary objective of getting 4 tower sums and 9 tower sums without boundary effects?

- Is it better to use 9 tower sums or 4-group sums of the 4 tower sums for triggering on jets? Is it easier and less expensive to do 300 of the 4-group sums than 1200 of the 9 tower sums plus the appropriate global sums?

5 Considerations in Proposed STAR EMC Level 0 Trigger

5.1 Dynamic Range for Trigger Independent of Readout

Consider using two levels of signals with limited dynamic range for each. Consider:

- 1% resistors for summing towers (if resistors are used at all)
- 1% or 5% capacitors for integrators
  1.5% rms gain uniformity in video amplifiers
- 53 dB to 60 dB (10^3 voltage ratio) common mode rejection
- 8 bit DAC's for trigger levels

First, look at constraints from AuAu events: Say a typical event with no jets puts 300 MeV into each of 1000 calorimeter towers. Both charged and neutral pions deposit all their energy in the nominal EM calorimeter. A 9 tower sum could have 2.7 GeV. Another consideration is the minimum level of high-P_t trigger in the high energy direct gamma or jet physics. This has been studied down to 3 GeV per tower.

Assume we make a break between the two scales at 3 GeV at the analog sum points. The levels described here are for individual towers as well as 4 tower and 9 tower sums. The sum of the 9 tower sums into a global sum may be done digitally to accommodate 10 TeV in a AuAu collision. The only problem I see in this scenario is that two towers of 1.6 GeV each might be buried in the electronic pickup noise for the high level trigger and would saturate the low level sum to look like 3.0 GeV. (remember that the low level signals are amplified by a factor before sending through a noisy environment for summing)

two 7 bit ranges	3 GeV/128 = 0.023 GeV min	3 GeV$\times$128=384 GeV max
two 6 bit ranges	3 GeV/64 = 0.05 GeV min	3 GeV$\times$ 64=192 GeV max
two 5 bit ranges	3 GeV/32 = 0.1 GeV min	3 GeV$\times$ 32=100 GeV max

It looks like two 5 bit ranges is fine for the trigger (ignoring problems of the boundary between the two ranges). This assumes that we are willing to duplicate many things at 2 ranges. The data readout will have to deal with very small signals but it won't have the same pickup with analog sum cables strung all over the magnet.

5.2 Other Trigger Dynamic Range Considerations

There are constraints on the dynamic range of the analog part of the trigger from the digital part. The 160 or so 9 tower sums are digitized and fed into XiLinx or similar Field Programmable adder trees. (We would like the field programmable feature to eliminate hot towers from the trigger.) The final sum cannot exceed 16 bits if it is to be used with other STAR trigger electronics. From global considerations, a 16 bit number which is the sum of something like 256 smaller numbers implies that the smaller numbers cannot have more than 8 bits. If we look in detail at implementing the sum with 3 layers of XiLinx 4003H chips, each of which have 3 internal layers of summing, we get 7 bits for the maximum for the input numbers if all chips are programmed identically.

As an example, a first layer chip has 3 layers of addition. Inside it, eight signals of 7 bits go to 4 of 8 bits, 2 of 9 bits, and one of 10 bits.(Fig. 5) In the second layer, eight signals of 10 bits go to one of 13 bits and in the last layer, eight signals of 13 bits go to the final one of 16 bits.(Fig. 6) If we implement the cable drivers and analog sums with video drivers, these seem to be gain matched to 2.5%. Consider the worst case where this is a flat distribution from -2.5% to $+2.5\%$. Then the RMS is 5%/root(12) or 1.44%. This is the resolution of a word with more than 6 bits, so 7 bits would be required to avoid having the digital resolution dominate.

We have to digitize a subset of the 9 tower sums. Flash ADC's of 8 bits are common. Eight bits of dynamic range at this point in the sum is consistent with at least 5 bits from each signal, and more like 6 or 7 if not all 9 signals are large simultaneously.

5.3 Dynamic Range for Readout Compared to the Trigger

We can tie down the low end of the readout as follows: We want to use muons for calibration to a couple of percent level. A Muon deposits energy in the scintillators by dE/dx to give the same signal as a 300 MeV electromagnetic shower. A muon goes through 20 layers of scintillator with 2 photoelectrons coming from each. It doesn't make much sense to have an ADC count very much less than a photoelectron for this purpose, so we get 40 ADC counts for a muon that looks like 300 MeV in the calorimeter. One ADC count is then 0.0075 GeV.

The nominal resolution of the EM calorimeter for real photons at 16%/root(E) is equal to the energy at .025 GeV. This is not quite right at this low energy but it gives a minimum ADC count within a factor of 3 of what we got with the muon consideration.

If we have a break between the two integrator scales at 3 GeV, (this is in the trigger, in the readout there is overlap rather than a break) it is at 3/.0075 or 400 ADC counts or about 9 bits. If we have 16 bits total, the maximum is 491 GeV per tower which is about a factor of 4 or 5 more than we expect to need for electrons from Z^0 with some production P_t and some resolution smearing and some background. Thus, the 3 GeV doesn't cause problems in this way.

5.4 Analysis of ADC Overlap for Readout

In order to learn about resolution, first consider using two 3-bit ADC's with a factor of 4 gain between the scales and no offset.(Fig. 7) The dynamic range is $2^3 \times 4$ or 5 bits. The amplified scale reaches 8 counts at a signal level which is at 2 counts on the unamplified scale. The next higher count on the unamplified scale then has 30% to 50% resolution, compared to 12% on the amplified scale.

Next consider using two 8-bit ADC's with a factor of 64 gain between the scales and no offset.(Fig. 2) The dynamic range is $2^8 \times 64$ or 14 bits. The amplified scale reaches 256 counts at a signal level which is at 4 counts on the unamplified scale. The next higher count on the unamplified scale then has 25% resolution, which is not good enough.

Next try two 10-bit ADC's with a gain of 16. The dynamic range is $2^{10} \times 16$ or 14 bits. The worst case resolution is 1.5%. 1/(1024/16). This is nice but the factor of 16 is not what we want for the trigger.

Next try two 10-bit ADC's with a gain of 32 between them. The dynamic range is 15 bits and the gain of 32 is OK. The worst resolution is 3% but this may be OK if it is at an energy where the calorimeter resolution is worse, namely below 28 GeV. This is OK since it can be put at emax/(10 bit-5 bit mult.) or about 3 GeV.

The circuit of a prototype dual integrator with two ADC's is shown in Fig. 8.

5.5 Analysis of Voltage Scales to Use

First we look at the trigger. Some fast differential amplifiers such as video amplifiers have input offset voltages of 2 mv. We would like this to be negligible compared to the signal with a 5 or more bit dynamic range, so say the minimum voltage is 10 mv and then the maximum would then be 320 mv for 5 bits, 640 mv for 6 bits and 1.28 volts for 7 bits. Another consideration is power consumption with 110 ohm differential pairs. 1 volt would give 9 mw dissipation in the receiver and perhaps in the driver also. With 40 thousand pairs, this could be 720 watts, or at least 1 kW with power supply inefficiencies. Actually, some existing driver chips use about 350 mw so the power in that case would be about 14 kW.

The most serious consideration is the absolute size of the EMI pickup from the high frequency Magnet SCR noise and the common mode noise from 5 to 65 volts ripple (from 400 volts) on the magnet coils at 720 Hz. If the cables were near the coils they would see a sizable fraction of this unless shielded twisted pair is used. There would be something like 150,000 feet of cable in 4 foot segments.

Next we consider the raw signals before integration. One photoelectron from the photo tube will get multiplied by the tube gain of something like 10^5. We will have to choose the gain carefully to get above noise in the integrator on the low end and avoid saturation/non-linearity at the high end. The photo tube might show saturation effects at 150 ma and the pulses might be 10 ns wide.

Hypothetically, the integrator noise might be 2 femto-coulomb so the dynamic range might be $1.5 \times 10^{-9}/2 \times 10^{-15}$ or 7.5×10^5 or around 16 bits. The buffer amplifier should not have noise more than 2 femto coulomb in 10 ns or 2×10^{-7} amps rms (at 80 MHz with a 2 ns rise time).

Actually, with my R-580 photo tube and a scintillator tile that gives about 1.5 photo-electron/mip I see signals after a x100 amplifier of 100 to 200 mv into 50 ohms. The pulses last about 10 ns baseline to baseline. The time jitter is something like 20 ns. The charge directly out of the tube is then 10^{-13} coulomb or 100 femto-coulomb. A dynamic range of 15 bits corresponds to raw signals from 1 mv to 32 volts or charges from 100 fc to 3 nc. The current at the high end would be 300 ma, which is in the non-linear region. The PMT in the calorimeter could have lower gain than this to reduce saturation. This should be done by using fewer stages, since the photo cathode efficiency is low at low voltage and the resolution would be worse at low voltage.

The voltages out of the integrators depend on the capacitor sizes and the gain of the buffer amplifier.

5.6 Pedestals, Offsets, Drifts

There are offsets and DC drifts at every stage of the readout and trigger. These cannot be eliminated by AC coupling because of the high and varying rates with monopolar pulses and high duty factors. We might consider bipolar pulse shaping, but let's consider a DC system first.

The charge integrator for photo tube pulses has an offset and a drift at the output. The desired range would be the maximum signal of 1 or 2 volts divided by the dynamic range of 10 bits (1024) or about 1 to 2 millivolts. The observed drift in the E880 version of the integrator with reset circuit was about 30 mV in one hour. This was primarily due to drifts in the power supply voltage. We may be able to get much smaller drifts with local voltage regulators and temperature control.

The next question is the overall offset of the differential driver circuit from the integrators to the trigger sums. With the proper differential receiver this may not matter much as long as it does not use up too much of the dynamic range. Perhaps we need identical current sources on each line of the differential cable to make it symmetric. One possible problem is the non-linearity of transistors with low base to emitter voltage. This can be solved by using the difference of two current mirrors as shown in Fig. 9. Probably the output transistor has to be biased to be in the class A amplifier region when the input is 0 volt with respect to ground of the integrator.

Next it may be useful to consider the receiver, the current sum, and the comparator as a group. One can consider several scenarios for this chain of functions. Let's look at three different ways to do the sums. The first two of these assume that the receiver chip produces signals with respect to the ground of the summer. First, in Fig. 10A use a good op-amp in a summing circuit and 1% resistors for each input to be summed. This would solve the offset and small signal linearity problems if we could find a fast op amp with good settling time for a reasonable price. There are only 2400 of these (or maybe 1200) so a few dollars each might be in the scope. Second, in Fig. 10B we could use a grounded base transistor for each input and tie the collectors together to make a current sum. In this case we have to worry about the offset of the emitter from ground if the base is really grounded or else use a negative voltage at the base equal to the emitter-base voltage. Third, in Fig. 10C use a differential output from the differential receiver and use two simple summers as in case 2, and take the difference. An op-amp or amplifier could take the difference. The best solution may be an amplifier with differential current output. One side can be tied to ground and the other to a summing resistor.

The next problem is the zero for the comparator with respect to ground and for the DAC which produces the threshold voltage with respect to ground.

5.7 A Solution to Many Problems: (it's all done with mirrors)

A new amplifier IC may solve several of these problems simultaneously. The Maxim Max435 differential Video amplifier has differential input, differential output, and the outputs can be wired together to sum the currents. The output is a differential current source driven by the difference in input voltage. This appears to solve the problems of differential driver, DC level, differential receiver, and analog sums. All this is done with no feedback so that it is claimed there is no phase shift or oscillation and the bandwidth is 275 MHz. The basis of this chip is said to be a current mirror in the output. I don't have the internal circuit, but my conceptual design of such a thing is shown in Fig. 9.

This can be used in conjunction with a special comparator. Some new comparators, also from Maxim, can work with 0 volts with respect to ground as the low end, even with single sided supplies. They also have internal latches and differential TTL or ECL outputs which can drive twisted pairs. At some location there must be a global digital "or" of these comparator outputs.

The problem with the MAX435 video chips is the power usage. At about 400 mw/chip, the total power used could be 7 to 14 kw. The frequency response is almost a factor of 10 better than we need for the integrated PMT signals, so perhaps a similar slower chip with much lower power requirements can be found or designed.

5.8 Uses for Analog Switches and Multiplexers

There are at least four areas where analog switches or multiplexers might be useful in this system:

1. We want to connect a cable to a scope to look at PMT signals, integrator outputs, trigger signals before comparators, etc. We need to do this while the experiment is operating. We cannot run very many cables. The use of analog multiplexers at places on boards where we can connect a high impedance load without causing reflections would accomplish this. The multiplexers would have to feed into a high impedance load like the input of a cable driver amplifier.

2. As mentioned in the introduction, if we have a good trigger, we do not need to put flash ADC's on every PMT. We can use switched capacitor arrays, SCA, for storage as done in the SVT, silicon vertex. This might have to be done on two levels, x 1 and x 32, if the dynamic range of the SCA were less than 14 to 15 bits. By using analog multiplexers, we can read out perhaps 8 photo tubes per flash ADC without stopping the clocking of the SCA. It is important not to stop clocking the SCA because the EMC data taking in this mode might be asynchronous with the trigger for the SVT or TPC. It would certainly be much faster, with events triggered perhaps once per couple of microsecond, and read in at perhaps a kilo-Hertz. One advantage of this method is the lower cost and simplicity of upgrading from 1200 photo tubes to 4800 in the barrel. We would have to choose the number of PMT per analog switch/ADC to allow a factor of 4 more inputs without timing problems.

3. If we only have money to build the trigger for one of the two levels, x 1 or x 32, analog switches could switch the system from one to another, depending on the physics requirements at the moment. The compromise here would be that one could not simultaneously do global patterns at low E_t and jet triggering in AuAu collisions.

4. Is there a way to program the gain of the amplifiers using analog switches? I think I have seen such circuits, but do they work at 100 MHz? This would be more graceful than a switch between x 1 and x 32.

5.9 Hot Channel Suppression

Every detector with a large number of channels has some defective channels, and in many cases these channels are "hot", pulsing at a very high rate. This is a particular problem in calorimeters with only one phototube per tower, so that no coincidence can be used. The causes may be light leaks, electrical discharge in the phototube, or electrical discharge in the base, or leakage of outside noise into the system. Or by failure of electronics, leaving a DC level on continuously. We need a way to selectively eliminate these channels from the trigger. This should be done by remote control from the counting house, and be modifiable for each data run of a few hours.

It should be easy to eliminate hot 9 tower sums by downloading different code to the Field Programmable Gate Arrays (Xilinx). This will kill 9 towers at a time and should be a last resort.

Since we intend to have analog multiplexers with input from every channel in order to look at the raw phototube signals or else the integrated signals, it may be a small perturbation to add an analog switch to each channel in the trigger to eliminate hot single channels. The readout would not be disabled.

5.10 Time budget

The purpose of the level 0 trigger is to select interesting events within 800 ns so that the TPC can be read out on each trigger without excessive dead time. The interaction rate may be 2×10^7 and the TPC may take 40 milliseconds to read, or 10 reads per second if we do not want excessive dead time.

The EMC electronics will be in crates in shielded boxes on the outside of the STAR detector. The diameter of the detector plus boxes is about 30 feet the half-circumference is then about 48 feet. The length is about 30 feet, ignoring the end caps. The routing of cables from the phototubes to the crates may be 10 feet. The total cable length involved is then over 90 feet. If the beta in twisted pair is 0.6, this is about 150 ns.

The digital part of the summing will be done in pipeline fashion. This involves 9 stages of summing, digital comparator, and final EMC trigger decision. There is also some combining of the EMC trigger with the other triggers to form a final trigger. We do not know the time needed for this, so a very crude time budget is as follows:

150 ns	cable propagation on the detector
370 ns	digital processing for EMC
40 ns	integration time for phototube signal
50 ns	analog settling time (comparator and amplifiers)
50 ns	cable from EMC to final trigger
100 ns	final trigger processing
800 ns	total time to trigger

5.11 Physical Placement of the Summers

Conceptually, this proposed trigger scheme would be very orderly with equal length cables everywhere if a summing card that does 1 tower, 4 tower and 9 tower sums is placed at each phototube.(Fig. 11) The cards would then be distributed over an area roughly 10 meters by 30 meters for the barrel, or 20 meters by 30 meters if there were two end caps.

There are several practical problems with this. It requires many cables to cross between phototube boxes along the length of the STAR detector, at least 7000 in the single scale version. It requires power distribution to 1200 locations.

There are also problems with another choice, doing the sums in, for example, VME crates at the ends of the phototube boxes near the ends of the magnets.(Fig. 12) Signals from the center 4 of the 20 phototubes along the z direction would have to go to both ends of the magnet, and all other signals would have to be delayed to match. Comparisons of the two situations are shown in Figs. 11 and 12.

It has been suggested that the summing could be done in crates at the center of the barrel on the outside of the iron. This would mitigate the problems for the barrel, but not for coupling the barrel and end cap. It is not yet known if space is available.

5.12 Cost Estimates for the Trigger Part

The cost estimate for the readout will be made elsewhere.

Here we consider the worst case of implementing the trigger on two scales a factor of 32 apart. If we can switch between Global Heavy Ion mode and High P_t mode, we only need half as many of most items. Or, if we can use the low end of the x 1 scale for the Global Heavy ion trigger a similar savings applies.

Nota Bene some of these prices are made up.

Video driver & receiver chips	
15 cables $\times$ 2 levels $\times$ 1200 towers = 36k cables $\times$ 2 chips per cable =72000 chips @ \$3 each (I got prices from the company)	\$ 216k
Comparator chips (analog)	
1200 9 tower sums $\times$ 2 analog levels $\times$ 3 trigger thresholds=7200 1200 4 tower sums... 7200 1200 single tower... 7200 21600 channels/4 channels per chip = 5400 chips @ \$6 each	\$ 32k
XiLinx chips	
20 at the input layer(160 signals/8 inputs) 3 at the intermediate layer 1 at the output layer mult by 2 for using two levels 48 chips @ \$250 each	\$ 12k
Digital Comparator	
2 of 16 bits or 8 of 4 bits 8 @ \$4	\$ 0.03k
Flash ADC (trigger, not readout)	
1200 towers $\times$ 2 levels 2400 chips 2400 @ \$10	\$ 24k
DAC chips (for trigger thresholds)	
3 thresholds $\times$ 2 levels = 6 chips @ \$10 (the real expense is in the fanout drivers)	\$ 0.06k
Cables and Connectors	
15 cables $\times$ 2 levels $\times$ 1200 towers =36k cables 150 k feet @ \$0.50/ft = \$ 75 k connectors 36 k $\times$ 2 ends @ \$2 = \$144 k (I have no idea what kind of connector)	\$ 219k
PC boards & connectors	
1200 local summing boards (with x1, x4, x9 at both levels on each. And with 32 twisted pair inputs, 16 twisted pair outputs, and 2 digital 8-bit outputs and 3 power leads and place for about 50 chips an a board.) 1200 @ \$50	\$ 60k
Power supplies	
try \$1 per watt @ 20 kW	\$ 20k

6 Hardware Prototypes at Argonne

Prototypes have been constructed of a multilayer XILINX digital summer and a fast analog current summer with good common mode rejection. A prototype of an integrator with integration on two scales a factor of 64 apart and a reset from each beam crossing was also built in CAMAC form. An integrator with shaping/subtraction of exponential tails instead of a reset was also built and used in an AGS experiment.

Timing tests on the digital summer showed that the clock frequency and total pipelining time were quite feasible for the proposed trigger. The digital test involved summing 8 words of 16 bits in 3 layers of two-word sums. The real trigger would have nine layers. The worst case for the three layers was 45 ns, so nine layers would take 405 ns. This summing is pipelined, so there is no problem with the 110 ns bunch crossing time.

The analog sums were done with a new kind of video amplifier, the MAX 435. This amplifier has good common mode rejection for noise suppression and the outputs can be wire -ored to make sums of a number of channels. The same video chip was used for differential cable drivers, receivers, and as a buffer to and current to voltage converter to use the summed current to provide a voltage to a MAX900 analog comparator.

One known problem with this implementation of the Analog sum is that the power requirement with these chips is too high. Since the frequency response is about a factor of 10 better than required for the integrated phototube signals, it may be possible to find another similar slower chip, perhaps CMOS, to do the same job with less power. A limitation may be the power dissipated in the termination of the twisted pair transmission lines. We used termination on both the driving and receiving ends, but this may not be necessary.

7 Acknowledgements

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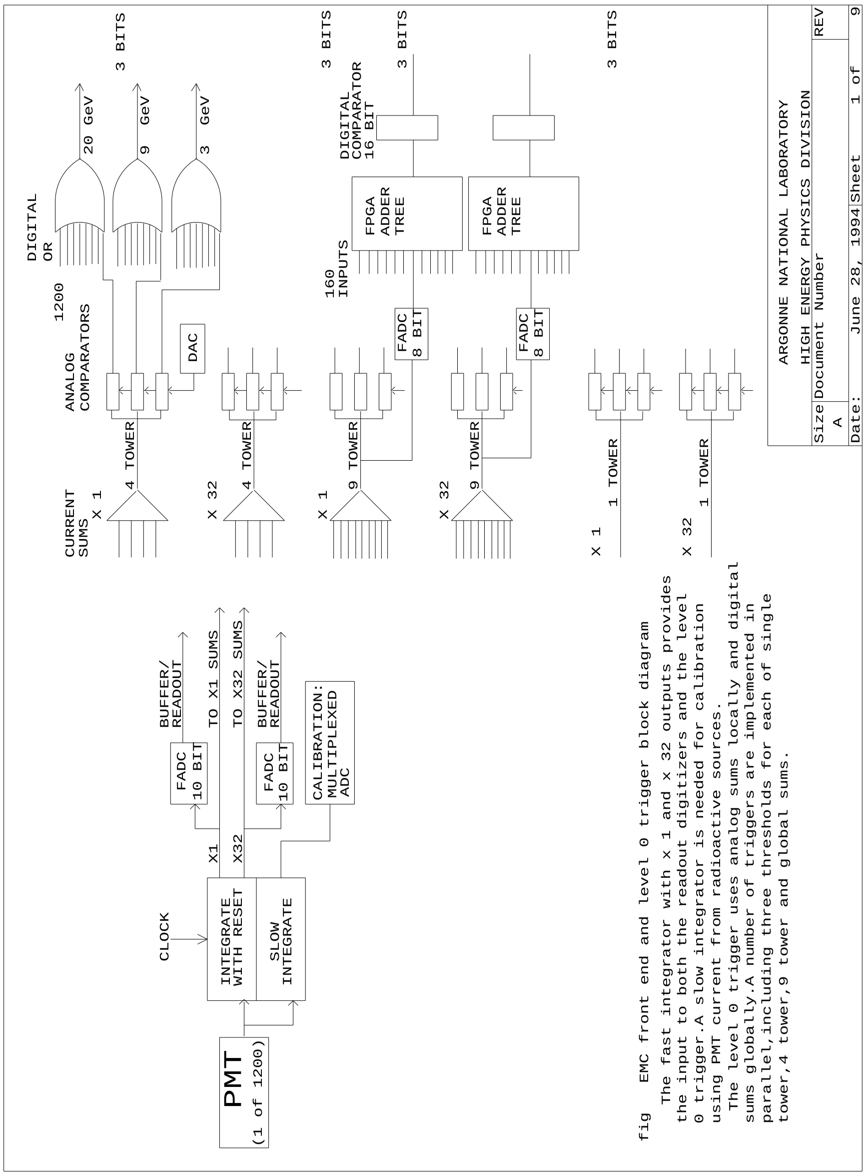

Figure 1: a) Block diagram of phototube signal shaping and signal distribution to readout and trigger and calibration. Fast integrators with x 1 and x 32 outputs provide the input to both the readout digitizers and the level 0 trigger. A slow integrator is needed for calibration using PMT current from radioactive sources. b) Block diagram of the proposed trigger scheme. The level 0 trigger uses analog sums locally and digital sums globally. A number of triggers are implemented in parallel, including three thresholds for each of single tower, 4 tower, 9 tower and global sums.

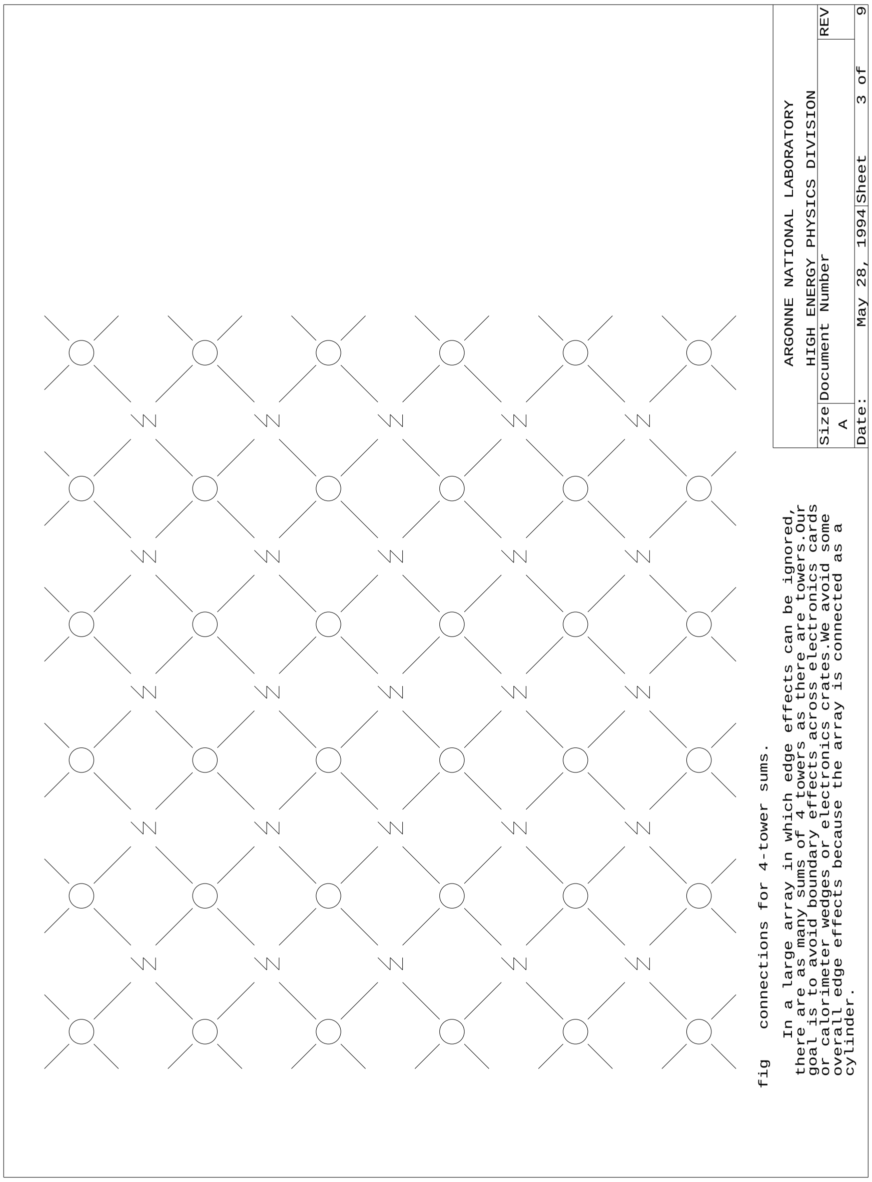

Figure 2: Connections for 4 tower sums. In a Large array in which edge effects can be ignored, there are as many sums of 4 towers as there are towers. Our goal is to avoid boundary effects across electronics cards or calorimeter wedges or electronics crates. We minimize overall edge effects because the array is connected like a cylinder for the barrel, and like longer cylinder if end caps are included.

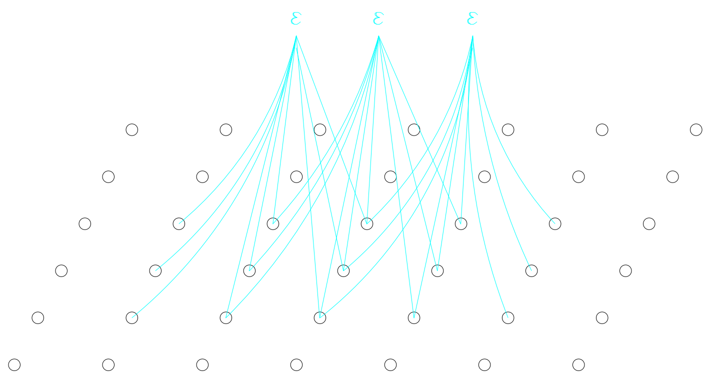

Figure 3: Connections for 9 tower sums. We need all possible 3 x 3 sums of 9 towers for the local trigger for jets. We use a non-overlapping subset to fan in for the global sum.

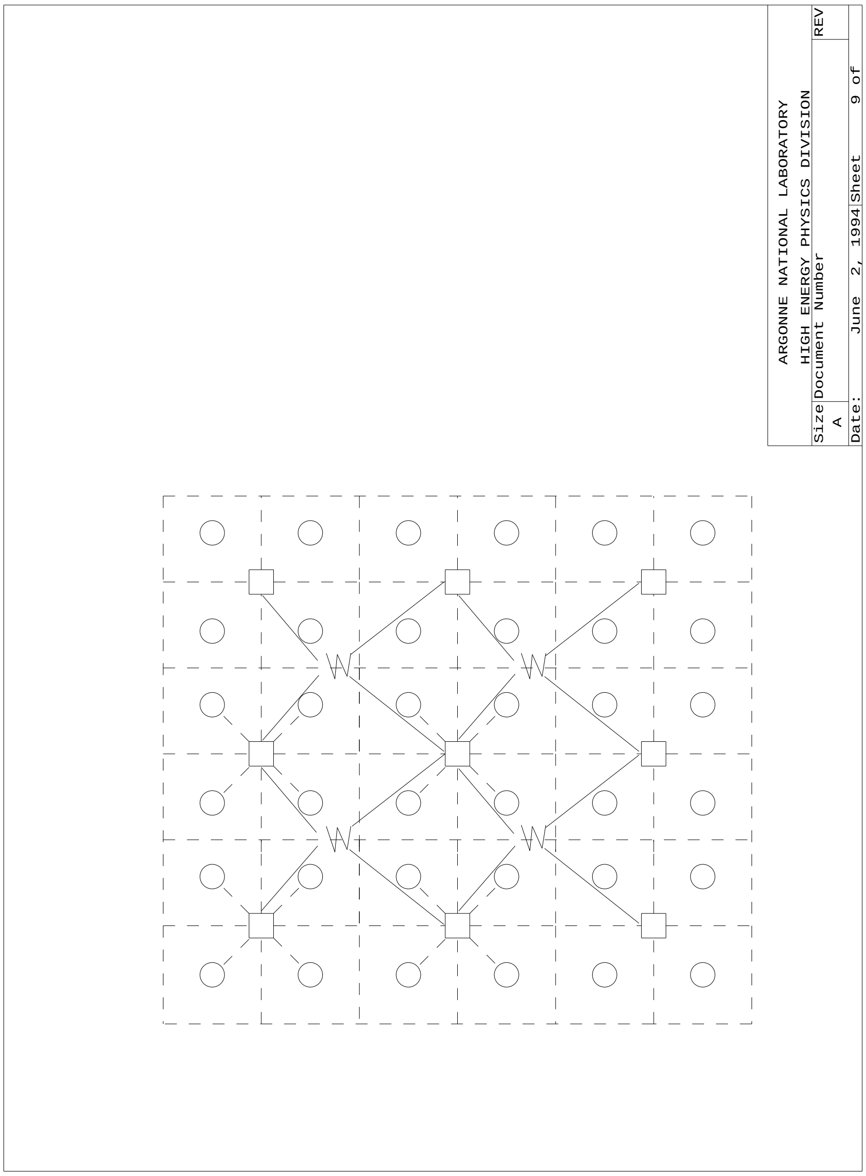

Figure 4: Connections for 16 tower sums. This is done with sums of 4 tower sums so that the wiring is simplified by a large factor compared to doing 9 tower sums.

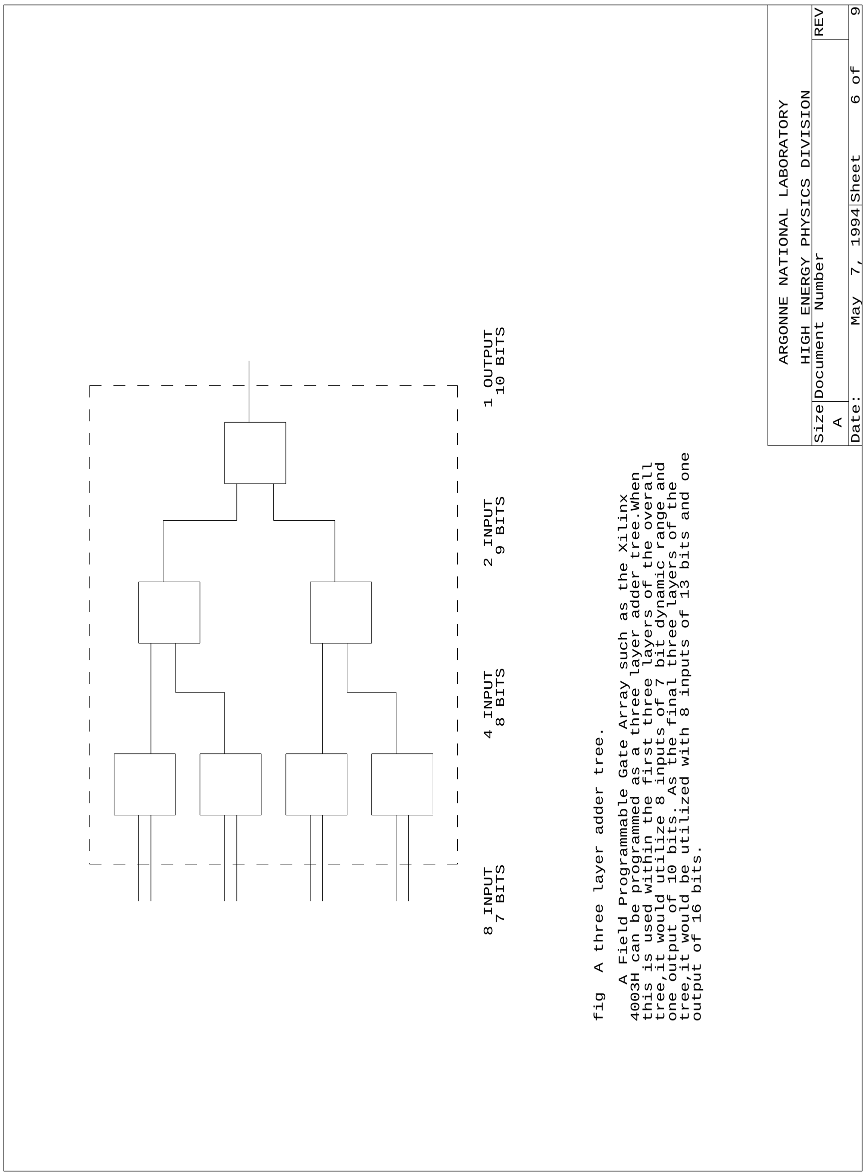

Figure 5: A three layer adder tree. A Field Programmable Gate Array such as the XiLinx 4003H can be programmed as a three layer adder tree. When this is used within the first three layers of the overall adder tree, it would utilize 8 inputs of 7 bit dynamic range and one output of 10 bits. As the final three layers of the tree, it would be utilized with 8 inputs of 13 bits and one output of 16 bits.

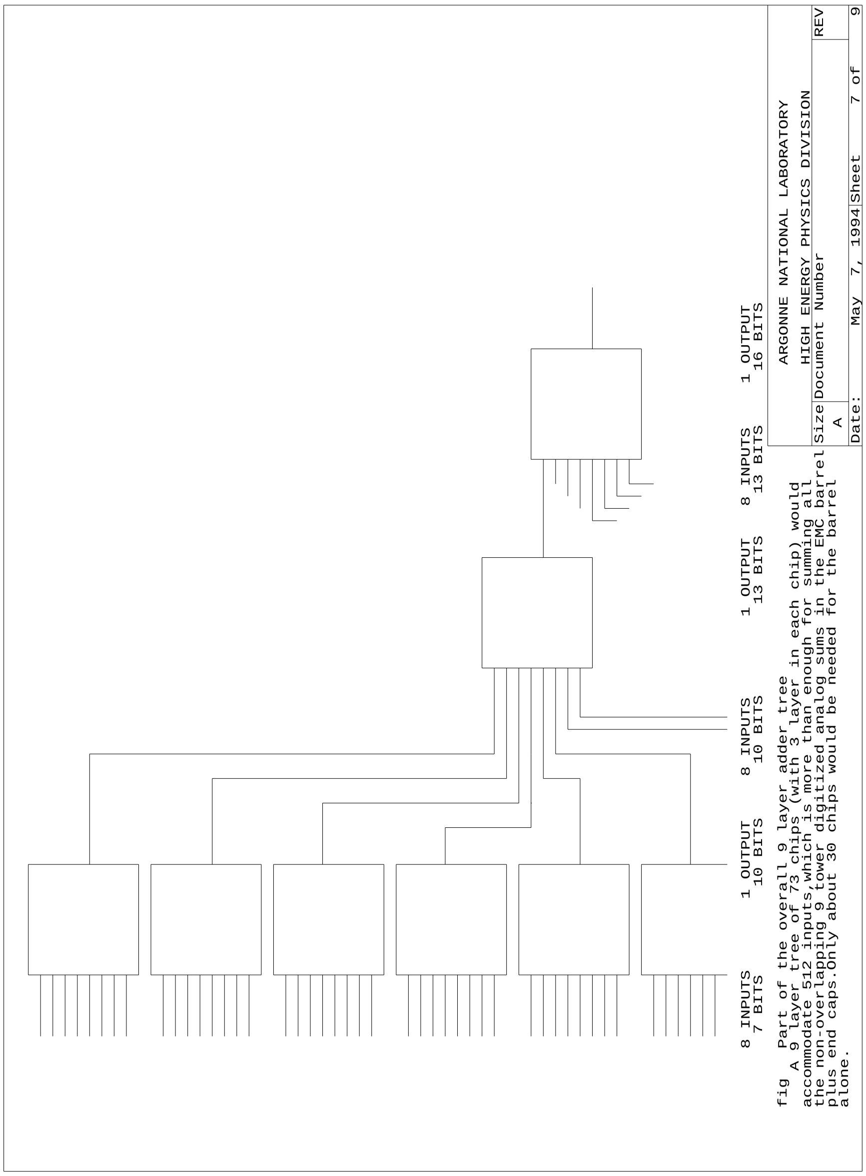

Figure 6: Part of the overall 9 layer adder tree. A 9 layer tree of 73 chips (with 3 layers on each chip) would accommodate 512 inputs, which is more than enough for summing all the non-overlapping 9 tower digitized analog sums in the EMC barrel plus end caps. Only about 30 chips would be needed for the Barrel alone.

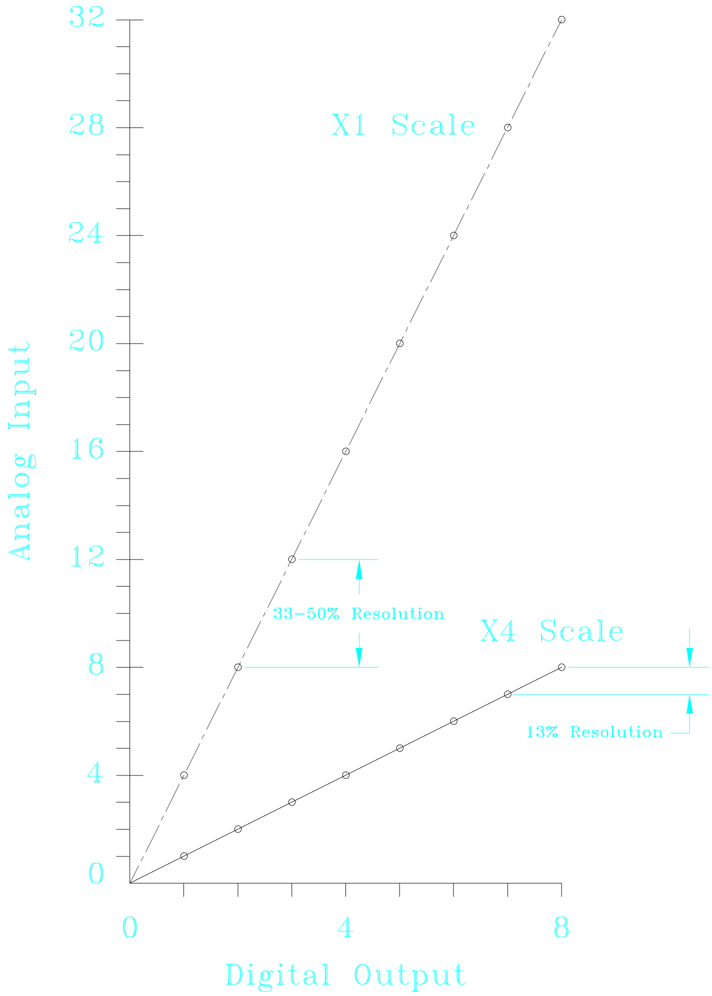

Figure 7: Example of resolution obtained with a simple dual-slope ADC.

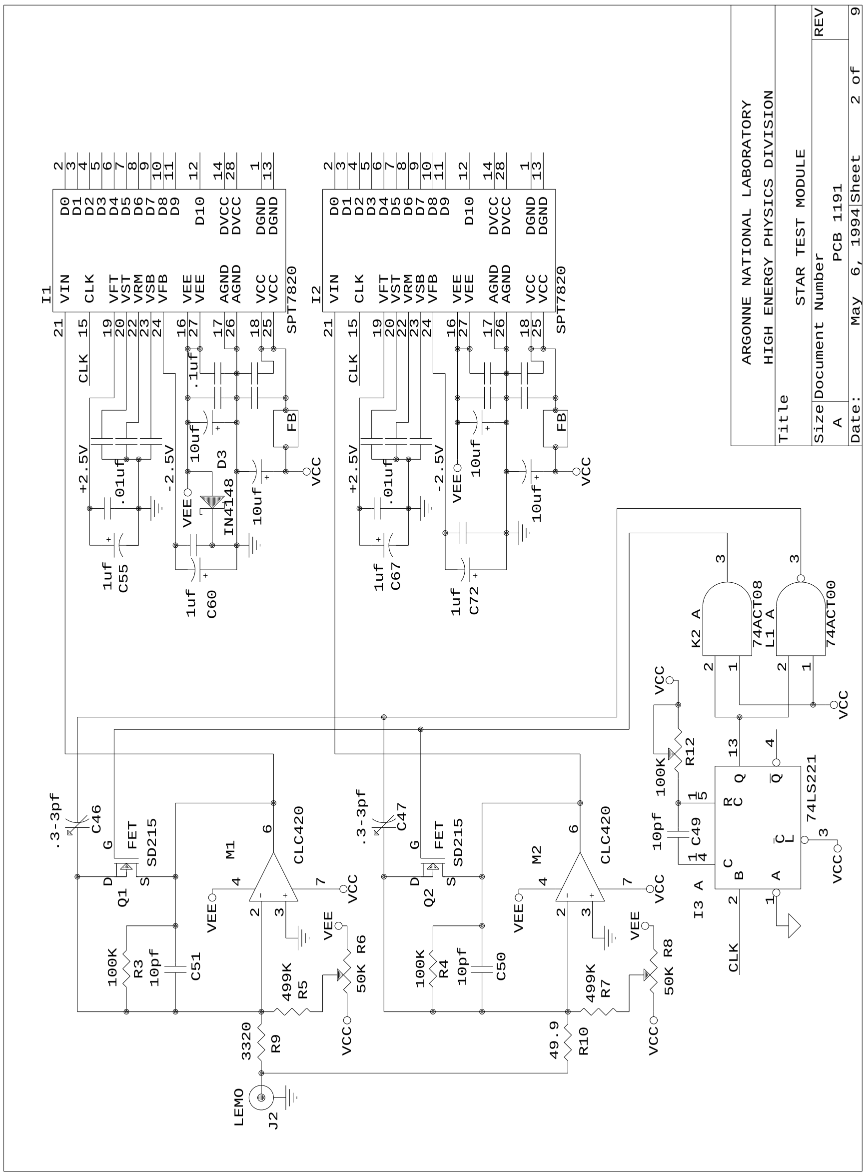

Figure 8: Front end of the gated integrator prototype built at ANL. Integration is done on two scales a factor of 64 apart in this version. The integrators are reset to zero by the beam crossing clock about 50 ns before each beam crossing. Flash ADC's of 10 bits are used on the output of each integrator. The very slow integrator needed for calibration with a radioactive source is not included.

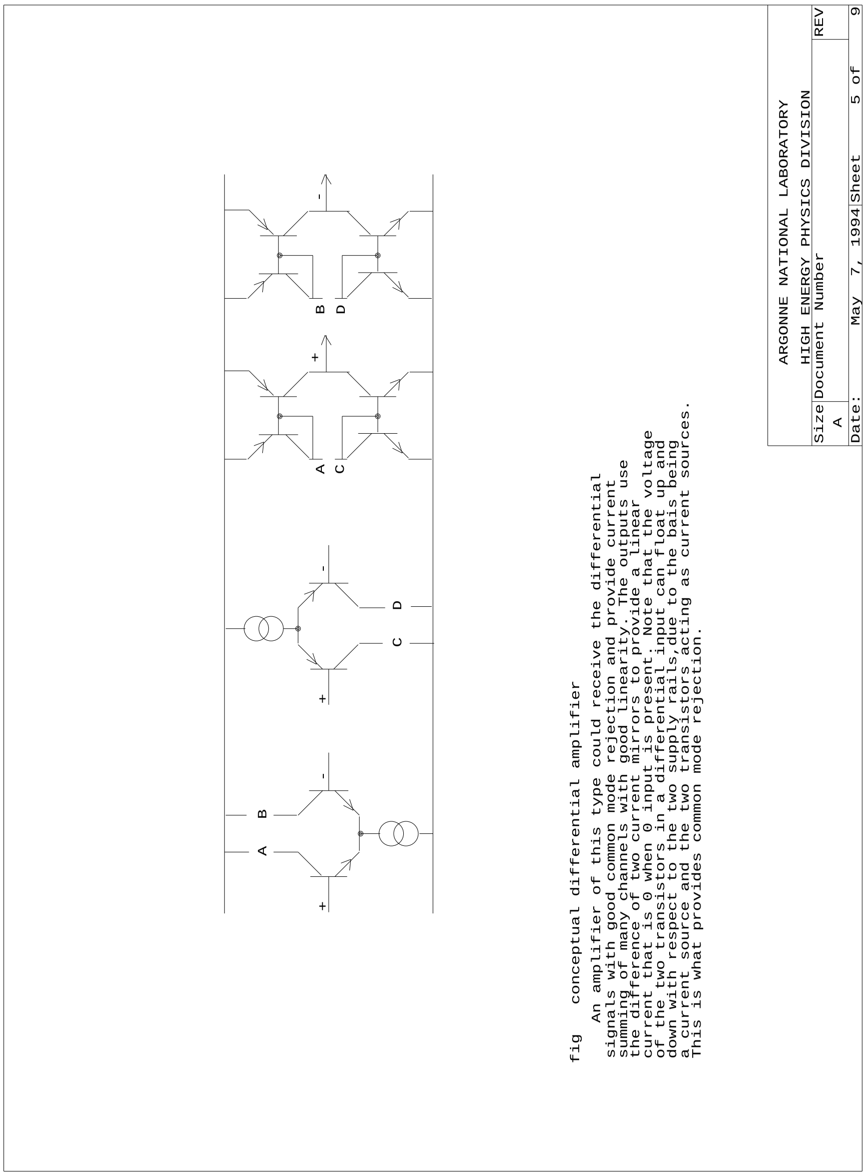

Figure 9: A conceptual differential amplifier. An amplifier of this type could receive the differential signals with good common mode rejection and provide current summing of many channels with good linearity. The outputs use the difference of two current mirrors to provide a linear current that is 0 when the input is 0. Note that the voltage of the two transistors in a differential input can float up and down with respect to the two supply rails, due to the bias being a current source and the two transistors acting as current sources. This is what provides common mode rejection.

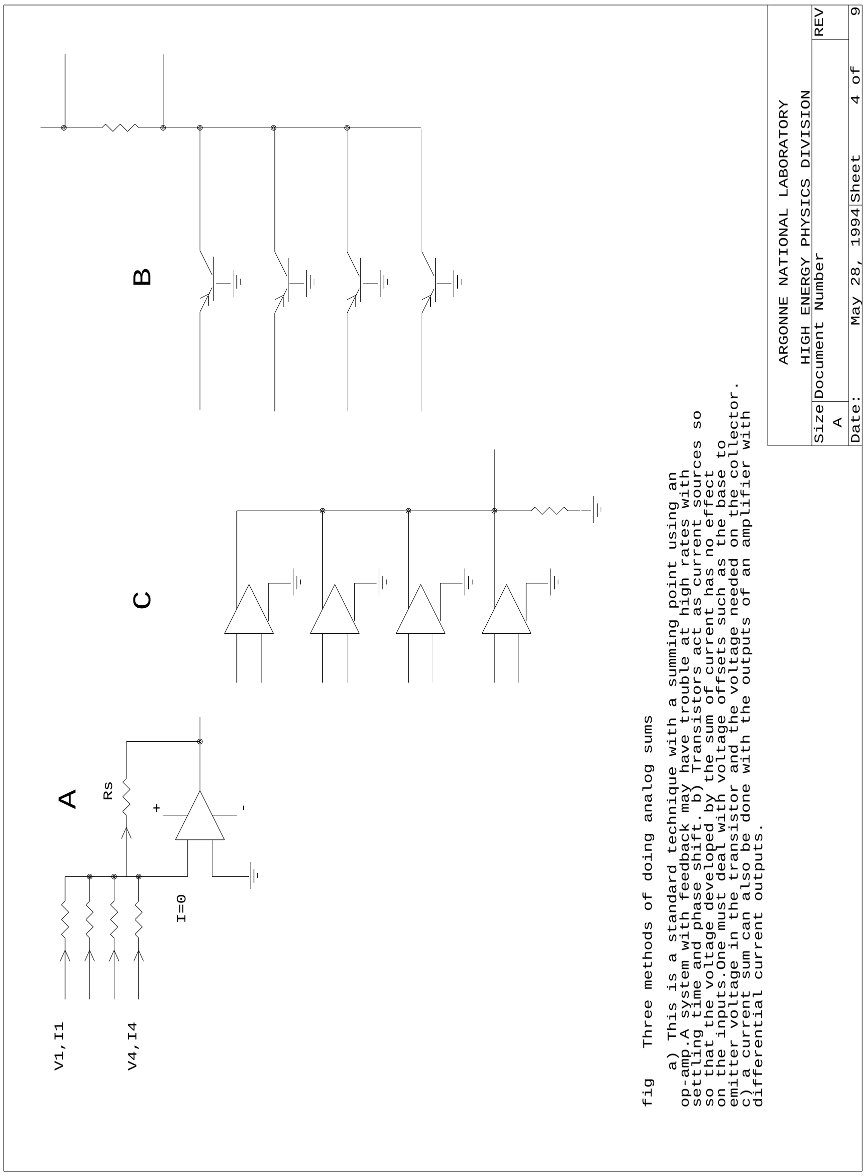

Figure 10: Three methods of doing analog sums. a) A standard technique is a summing point utilizing an op-amp. Such a system may have trouble at high rates with settling time and phase shift. b) Transistors act as current sources so that the voltage developed by the sum of the currents in a resistor has almost no effect on the inputs. One must deal with offset voltages such as the base to emitter voltage in the transistor and the voltage needed on the collector. c) A current sum can also be done with the outputs of an amplifier with differential current outputs.

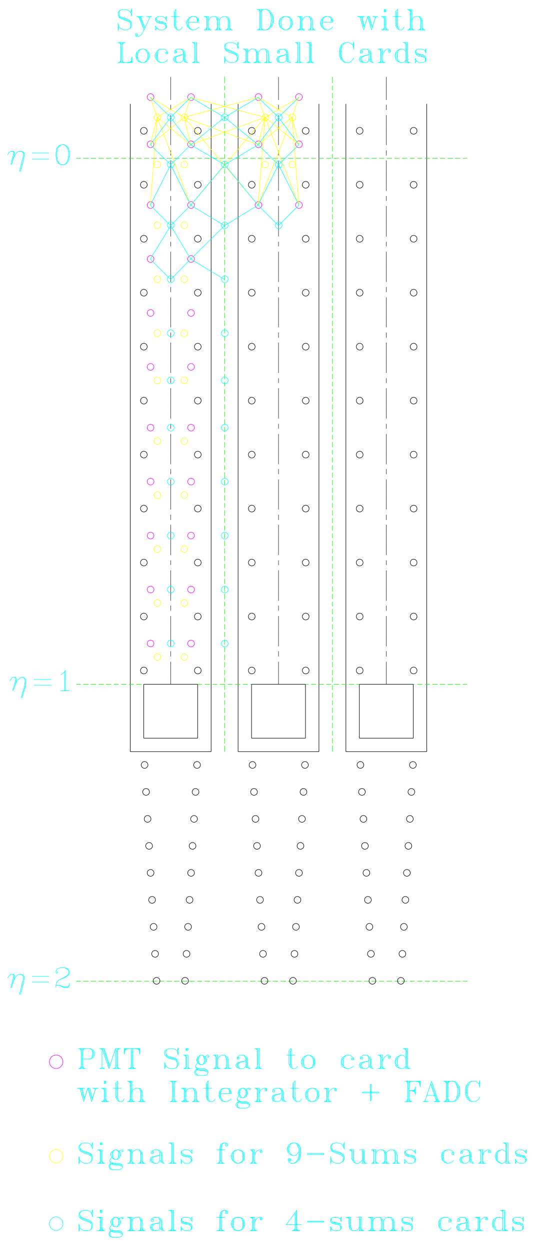

Figure 11: Topology and cables on the outside of the STAR magnet for a system done with local summing cards. We assume boxes for the phototubes and readout crates on the back of each of the 30 magnet flux return bars. For each phototube there would be a small card with two integrators, two flash ADC's, and analog summing and comparators for 1 tower, 4 tower, and 9 tower sums. About 1/9 of the cards would also have a FADC for feeding into the digital part of the trigger for the global sum. There would be about 40 twisted pairs across the gap between boxes for the 4 tower sums, and approximately 120 pairs for the 9 tower sums.

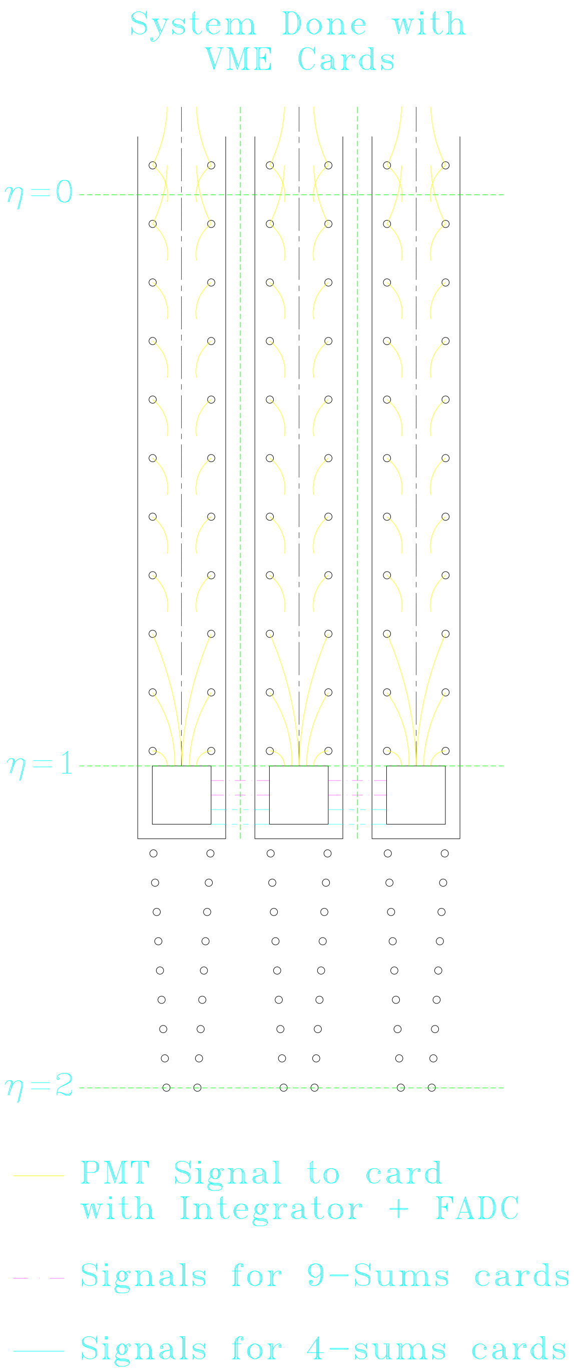

Figure 12: Cable routing for a system done with summing cards in crates on the ends of the phototube boxes. One problem is that the center 4 phototubes in each row of 20 must have cables to both ends of the detector. It has been suggested that putting summing crates at the center of the detector might be a better approach. Note that the timing from all phototubes (including End Caps) to the summing points must be equalized.