A Low Noise Amplifier-Shaper with Tail Correction for the *STAR* Detector

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Abstract

A 16 channel low noise amplifier shaper has been designed for the STAR particle detector of the RHIC accelerator. The STAR Amplifier-Shaper (SAS) includes a pole/zero network which cancels the long tail of the Time Projection Chamber (TPC) signal. The tail correction can be adjusted depending on the type of gas used in the TPC.

The SAS equivalent noise charge is $900e^{-}_{rms}$ with 25pf detector capacitance (the test board having 7.7pF of parasitic capacitance), and with 80ns shaping time (step response). The measured noise slope is $13.7e\text{-}_{RMS}$/pF. The shaper pulse FWHM is adjusted at 180ns (detector response) with +/-4% variation over the entire dynamic range. The shaping time and the tail correction are adjusted with external voltages using MOS resistors. The gain is 16mV/fC with a linearity of 4%. The crosstalk is about 0.36% which have a negligible effect on the position resolution. The circuit also includes an on-chip calibration system in which the test input charge is controlled by a DC voltage. The output buffer drives a 2V swing on 50pF output load for a total power consumption of less than 750mW (+/-5 Volt supply). On-chip protection diodes have also been integrated.

The full custom chip has been integrated in the CMOS ORBIT 1.2µm technology with double polysilicon capacitors.

I. INTRODUCTION

The Solenoidal Tracker at RHIC (STAR) is a nuclear detector being built to study high energy heavy ion collisions at the Relativistic Heavy Ion Collider (RHIC). Charged particles are tracked by a Time Projection Chamber (TPC) in which the electrons drift to the two end-caps where the signal is multiplied by anodes wires and detected on a pad. The minimum ionizing signal (MIP) is around 19,000e- or 3fC. Monte Carlo studies indicate that a 20:1 signal to noise ratio is needed to reach the required position resolution. The TPC electronics [1], is implemented in two custom integrated circuits, the analog front-end SAS and the waveform digitizer SCA/ADC (Switched Capacitor Array/ADC, [2],[3]).

The electronics requirement for the SAS is mainly to achieve low noise amplification and tail cancellation. The detector pads vary between 8pF to 30pF (15pF average), depending on the length of the trace to the front-end board. The TPC gas will be either P-10 or He-Eth. These two gas have different electron drift time requiring the SAS to have adjustable tail correction and shaping time. Each channel is connected to 2 SCA/ADCs which correspond to an output load of 50pF. Other specifications include linearity better than +/-5%, crosstalk less than +/-0.3% for space resolution, power consumption of less than 50mW/channel and DC output voltage matching within +/-100mV across all devices.

II. FRONT-END ARCHITECTURE

Figure 1 shows the SAS architecture. It consists of a low noise integrator with a reset switch, followed by a shaper amplifier and a buffer stage. The integrator is a folded cascode optimized to minimize its noise contribution for an input capacitance of 30pF. The input transistor's transconductance is about 33mA/V and represents about 100% of the total noise.

The reset is implemented using a CMOS switch and dummy-switches to reduce the charge injected on the integrator capacitor (C_f=1.6pF) when releasing the reset. The reset signal is brought on chip as differential voltages of about 100mV to reduce the clock feedthrough.

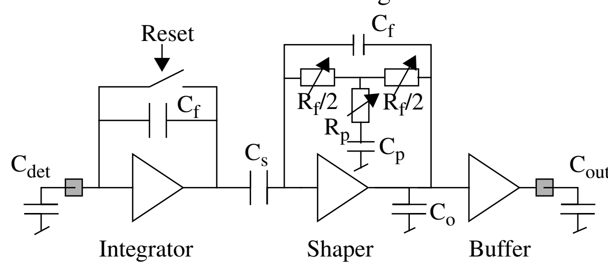

Fig1.: SAS block diagram

The shaper amplifier uses the 'cold resistor' technique for the differentiation stage. Its equivalent noise is reduced by the close loop gain compared to a real RC differentiation:

$$R_{diff} = \frac{1}{g_m}\left(\frac{C_o + C_f}{C_f}\right) \tag{1}$$

where g_m is the shaper's input transistor transconductance corresponding to the main shaper's noise contribution.

Large resistors are difficult to implement in integrated circuits. Well diffusion have the largest sheet resistance (1-2 kOhm/square) but are known to induce parasitic effects due to their voltage dependency and their associated parasitic capacitance affecting the linearity and the crosstalk [4], [5]. Resistors required for the integration pole R_fC_f and the tail cancellation network R_pC_p have been implemented using a MOS resistor (fig.2). MR is biased in its linear (or Ohmic) region by M_1 and M_2.

The resistor value controlled by the external voltage V_R is given by:

$$R \approx \frac{1}{\beta(V_R/2 - V_T)} \tag{2}$$

V_T being the threshold voltage of M_R and $\beta=\mu_o C_{ox} W/L$.

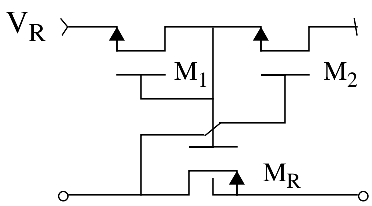

Fig.2: MOS resistor

The linearity of the MOS resistor is limited in voltage range, usually much less than a volt. The shaper's feedback resistor has been implemented with 4 MOS resistors in series, reducing the voltage across each resistors for a better linearity. The area used by the MOS resistors is very small compare to what it would have been using a well resistor.

The buffer has been designed to drive more than 50pF without any distortion and provide some additional gain. It has a separate power supply to avoid any feedback of the signal to the low noise front-end. Its power consumption is about 70% of the total power for one channel.

III. Tail cancellation

The gas used in the TPC will be either P-10 or He-Eth. The signals arising from the avalanche region is approximated by a 1/t relationship shown in figure 3, [6]. The measured TPC signal can be fitted by the sum of 3 exponential terms expressed in equations 3 and 4 for P-10 and He-Eth respectively:

$$i(t)_{P-10} = I_o\left[26.8e^{\frac{-t}{20.9ns}} + e^{\frac{-t}{287ns}} + 0.1e^{\frac{-t}{2.28\mu s}}\right] \tag{3}$$

$$i(t)_{HeEth} = I_o\left[7.4e^{\frac{-t}{43ns}} + 4.28e^{\frac{-t}{114ns}} + 0.3e^{\frac{-t}{755ns}}\right] \tag{4}$$

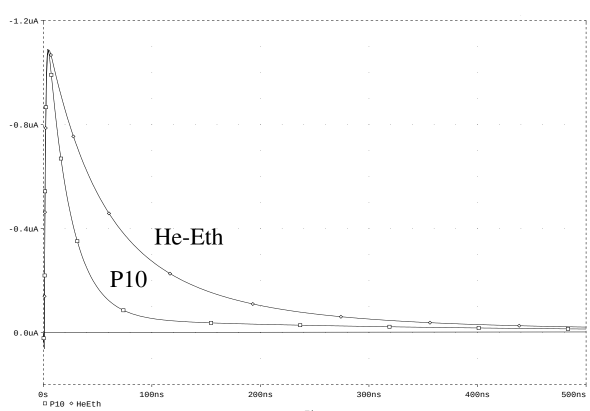

Fig.3: TPC signal for P-10 and He-Eth.

The signal function in the time domain can be expressed by:

$$i(t) = i_o(t) * h(t) \tag{5}$$

$i_o(t)$ represents the initial impulse charge (unit step response) and h(t) the signal transfer function corresponding to the sum of the exponential terms in 3 and 4. In the Laplace domain, the transfer function is:

$$H(s) = \mathcal{L}\{h(t)\} = \left[\frac{A_1}{1+s\tau_1} + \frac{A_2}{1+s\tau_2} + \frac{A_3}{1+s\tau_3}\right] \tag{6}$$

Cancellation of the tail of the TPC signal can be realized by deconvolution filtering technique [6]. It has been implemented as a pole/zero T bridge network in the shaper's feedback loop with C_p and R_p in figure 4.

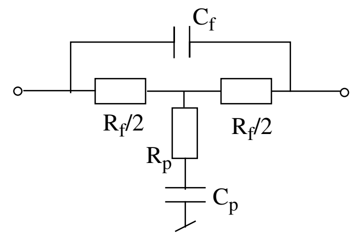

Fig.4: Pole/zero T bridge network

The feedback transfer function can be approximated by:

$$H_f(s) \approx \frac{(1+s\tau_f)}{(1+s\tau_p)} \tag{7}$$

where $\tau_f \sim C_f R_f$ and $\tau_p \sim C_p R_p$.

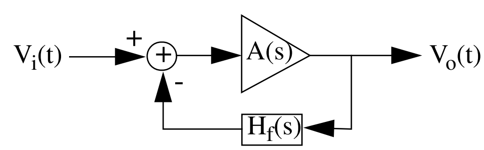

Fig.5: Negative feedback configuration

The feedback configuration as shown in figure 5 gives the global transfer function:

$$\frac{V_o}{V_i} = \frac{1}{\frac{1}{A(s)} + H_f(s)} \approx \frac{1}{H_f(s)} \tag{8}$$

A(s)>>1 is the open loop transfer function of the amplifier.

The response of this network to the signal H(s) in the Laplace domain is given by:

$$V_{so}(s) = I_o\frac{(1+s\tau_p)}{(1+s\tau_f)}\left[\frac{A_1}{1+s\tau_1} + \frac{A_2}{1+s\tau_2} + \frac{A_3}{1+s\tau_3}\right] \tag{9}$$

The time constant τ_p is adjusted for $\tau_p=\tau_3$, cancelling the pole τ_3 corresponding to the long tail of the signal ($\tau_3>\tau_2>\tau_1$). Figure 6 gives the SAS response to a generated P-10 signal. The remaining signal has less than 1% tail remaining after 1µs. The value of R_p is controlled externally to adjust the tail cancellation depending on the gas used in the TPC.

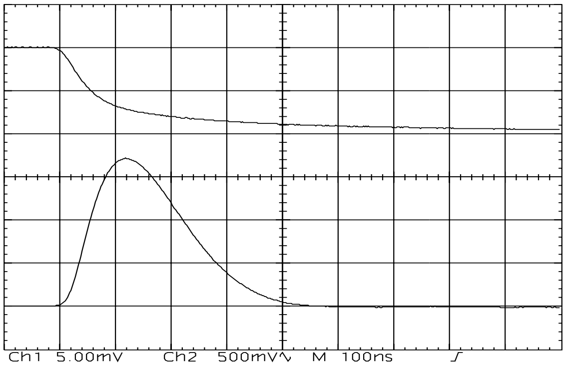

Fig.6: Integrator and shaper output response for P-10

IV. SAS PERFORMANCES

The over-all SAS gain is 16mV/fC (+/-2.5% across all chips). The integrator dynamic range is more than 2.5pC corresponding to 820 times the minimum ionizing signal.

The change in pulse shape with the amplitude, expressed by the FWHM, is within +/-4%. The shaping can be adjusted externally by a DC voltage controlling R_f, therefore the integration time constant C_fR_f, and with the shaper's bias current controlling the input transconductance g_m (i.e. R_{diff}, equation 1) hence the differentiation time constant C_sR_{diff}. The shaping can be adjusted from 60ns to 150ns peaking time (delta function response), fig.7, corresponding at 90 to 190ns in response of the P-10 input signal, fig.8.

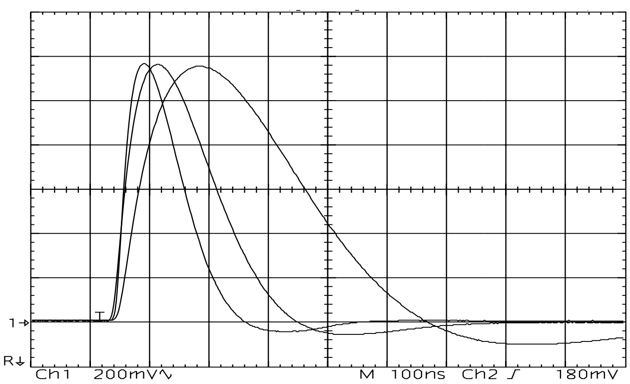

Fig.7: SAS shaping control (delta function input)

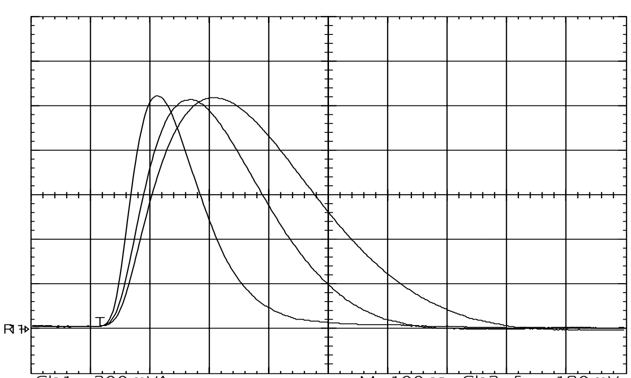

Fig.8: SAS shaping control (P-10 signal input)

The noise has been reduced to the limit obtainable with a CMOS technology for those large detector capacitance of up to 30pF. The noise slope can be calculated using the equivalent noise charge (ENC) relation of a RC-$(CR)^2$ filter:

$$\frac{ENC}{C_{IN}} = \sqrt{\left[\frac{e^2}{2}KT\frac{2n}{3g_m}\frac{1}{\tau}\right]\frac{1}{q}} = 13.8\frac{electron}{pF} \qquad (10)$$

with g_m~33mA/V (PMOS=7,000/1.2 at 5mA), the inversion slope n~1.3 and a shaping time constant of τ=80ns (i.e. peaking time). The input transistor noise contribution represents about 100% of the thermal noise, equivalent to the noise slope (equation 10).

The equivalent noise charge measured (ENC in e^-_{rms}) is $560e^-$ + $13.7e^-$/pF (referred to the input); the total parasitic capacitance of the test board was 7.7pF.

An on-chip calibration system has also been integrated as shown in figure 9. Any channel or pattern of channel can be selected via a shift register (chips can be daisy-chained). The calibration charge is set by an external DC voltage. The calibration capacitance is first grounded and then switched to the DC voltage, via the CAL signal, injecting the charge $Q=V_{DC}.C_{CAL}$. The test capacitance C_{CAL} is 0.1pF. The integral linearity of the calibration system is around +/-1%.

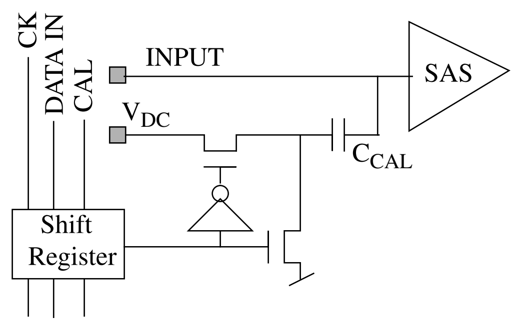

Fig.9: On-chip calibration

The crosstalk measured between channels is better than +/-0.36% which will not affect the position resolution. The DC output voltage measured for 16 channel on different chips is within +/-100mV measured across all chips.

Gain	16 mV/fC
Linearity	<4%
Internal Calibration	+/-1%
Maximum output voltage swing	2 volts
Integrator dynamic range	> 2.5pC
Shaping time (i.e. peaking time)	60 to 150 ns
Tail correction	0.5 to 2 µs
FWHM variation	< +/-4%
Crosstalk	< +/-0.36%
Equivalent Noise Charge in e^-_{RMS} (T_P=80ns, C_{BOARD}=7.7pF)	$560e^-$+$13.7e^-$/pF
Total power consumption (16 channel)	< 750 mW
Output load	50 pF
Die size	2.6 x 3.6 mm^2

Table 1: SAS performance

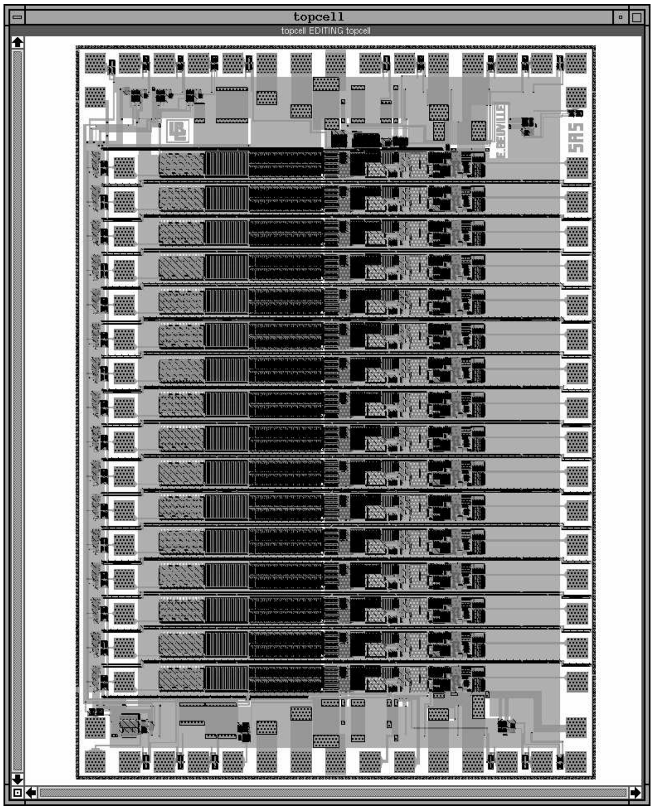

Fig.10: The SAS chip (2.6 x 3.6 mm^2)

V. Production testing

The STAR TPC has 136,600 pads. Nearly 9000 SAS chips will be required to instrument the TPC (8% are already in production). We expect a yield of about 70%. The SAS produced will be wire bonded in a plastic chip carrier and tested in a custom-build chip tester. The power consumption, gain, noise, crosstalk and signal FWHM are measured in 1 minute. Chips are individually labeled with a bar code to keep track of the testing procedure.

VI. Conclusion

The STAR Amplifier Shaper (SAS) is a 16 channel amplifier shaper designed for the STAR TPC, fig.10. Its performance is summarized in table 1. The circuit has been optimized for the TPC of the STAR detector with detector pads from 8 to 30pF. The shaping time constant and the tail cancellation are controlled externally giving some flexibility in the choice of the gas to be use in the TPC. The SAS noise contribution is reduced to the minimum achievable with the CMOS technology. The on-chip calibration circuit allow to test the functionality of all channels in any desired pattern with a good resolution.

The SAS integrated circuit seems well suited also for many other multielectrode devices. The total power consumption of the chip can be considerably reduced if the output load of the chip is reduced (the buffer stage being the main contribution: 70% of the total power consumption).

VII. Acknoledgement

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VIII. References

[1] S.R.Klein *et al.*, “The STAR TPC Front End Electronics”, *these proceedings*.

[2] S.A.Kleinfelder, “A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit”, *IEEE Trans. Nucl. Sci.* **37**, 1990, p1230.

[3] O.B.Milgromme and S.Kleinfelder, “A Monolithic CMOS 16 Channel, 12 Bit, 10µs Analog to Digital Converter Integrated Circuit”, *IEEE Trans. Nucl. Sci.* **40**, 1993, p721.

[4] E.Beuville, S.Buytaert, C.Cerri, P.Jarron, “Low Noise Analog CMOS Signal Processor with a Large Dynamic Range for Silicon Calorimeters”, *Nuclear Physics* B (Proc. Suppl.), **23A**, 1991, p198.

[5] E.Beuville *et al.*, “AMPLEX-SiCAL: a Large Dynamic Range Low-Noise CMOS Signal Processor for Silicon Calorimeters”, *IEEE Trans. Nucl. Sci.* **NS-39**, 1992, p.766.

[6] R.A.Boie, A.T.Hrisoho, P.Rehak, “Signal Shaping and Tail Cancellation for Gas Proportional Detectors at High Counting Rates”, *Nucl.Instr. and Meth.* **192**, 1982, p365.