STAR Note # 239

Front End Electronics for the STAR TPC

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Abstract

The Solenoidal Tracker at RHIC (STAR) is a large acceptance detector now being built to study high energy heavy ion collisions. It detects charged particles with a large time projection chamber. The 136,600 TPC pads are instrumented with waveform digitizers, implemented in custom low noise preamplifier/shaper and switched capacitor a array/ADC's ICs. The system is highly integrated with all analog functions mounted on small cards that plug into the TPC. Detector mounted readout boards multiplex data from 1152 channels onto a 1.5 Gbit/sec fiber optic link to the data acquisition system.

1 INTRODUCTION

STAR[1] is a large solid angle detector now being built to study high energy heavy ion collisions at the Relativistic Heavy Ion Collider (RHIC). RHIC will collide ions ranging from protons up to gold (including dissimilar species) at center of mass energies up to 200 GeV/nucleon. Scheduled for initial operation in 1999, STAR, shown in Figure 1, will be composed of a silicon vertex tracker, large TPC to track charged particles with $|\eta| < 2$, time of flight system, electromagnetic calorimeter, and forward tracking TPC, all in a 5 kG solenoidal magnetic field.

Because of the extremely high charged particle multiplicity, three dimensional space point readout is required for track reconstruction. STAR uses a pad readout TPC to obtain 3 dimensional point data. The TPC is 4 meters long, and extends radially from 50 cm radius out to 2 meters. A charged membrane is placed in the center, and electrons drift to the two endcaps, where the signal is multiplied by anode wires. The image charge is detected on 136,600 pads arranged in 45 rows on the two endcaps.

Each TPC pad is instrumented with a 512 sample waveform digitizer, dividing the TPC into 70 million space points.

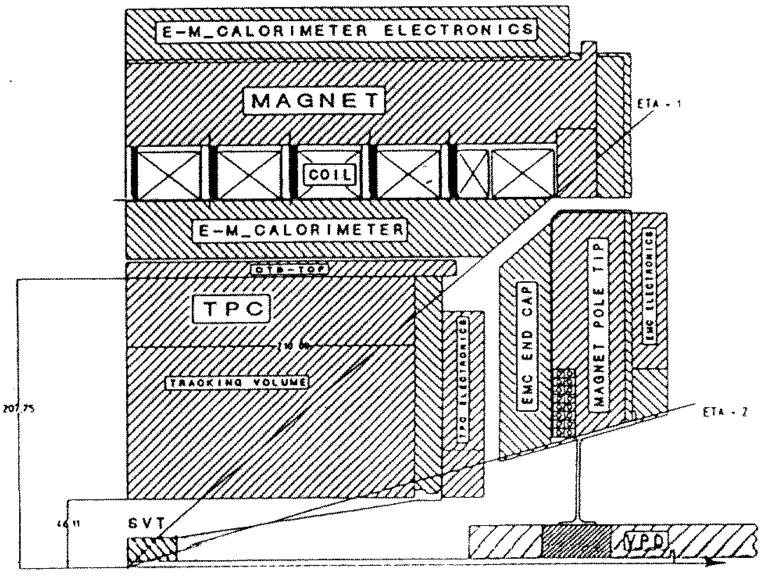

Figure 1. A quarter section view of the STAR detector.

The STAR electronics benefits from previous experience with the NA- 49[2] and EOS[3] TPC electronics. STAR follows the pattern set by these detectors with a preamplifier/shaper, switched capacitor array, with the electronics mounted on the detector. One major difference between STAR and it's predecessors is the data bandwidth; to provide an acceptable rate into the level 3 trigger, this data must be digitized and read out at up to 200 Hz.

2 ELECTRONICS REQUIREMENTS

The TPC gas will be either 90% argon, 10% ethane (P-10), which will have a 50 msec drift time, or 50% helium- 50% ethane, with an 80 msec drift time. The pads on the inner 13 rows measure 2.85 mm by 11.5 mm, while those on the outer 32 rows are 6.2 by 19.5 mm. The pad capacitance's range from about 8 pF to over 30 pF (15 pF average), depending on the length of the trace to the FEE card connector.

Each of the 512 time samples corresponds to a 4 mm drift distance. Diffusion and electron statistics limit the resolution in the drift direction to about 700μ, or about 1/5 of a time ample. In the azimuthal direction, the limit is 280/410 μ (inner/outer pad rows), determined by charge sharing among neighboring pads. Monte Carlo studies indicate that to reach the detector resolution limit, a 20:1 signal to noise ratio is required. The dynamic range is set by the requirement that the electronics accommodate a 200 MeV/c proton, which has about 10 times a minimum ionizing signal. To allow for Landau fluctuations, the electronics must not saturate for signals up to 40 times minimum ionizing.

3 ANALOG ELECTRONICS

The overall signal flow is shown in figure 2. The analog circuitry is implemented in two custom integrated circuits, the SAS (STAR preAmplifier /Shaper) and the SCA/ADC (Switched Capacitor Array/ADC). Both chips are 16 channels wide, and implemented in Orbit 1.2 μ CMOS.

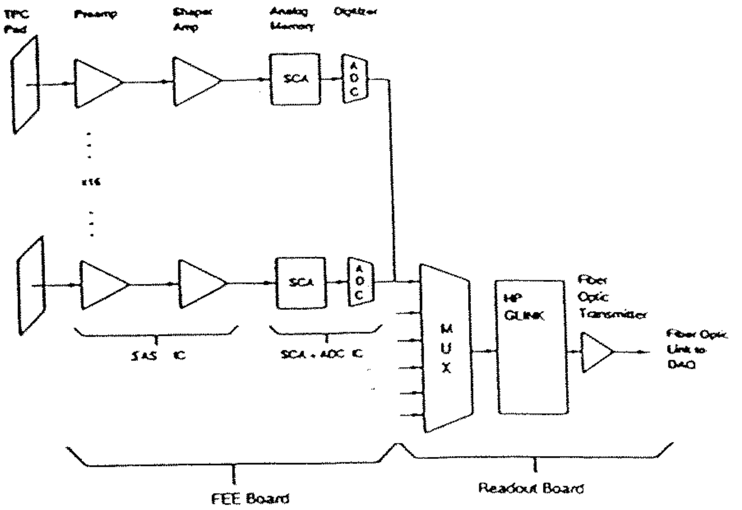

Figure 2. The FEE signal processing chain.

The SAS chip[4] incorporates an integrating preamplifier with switched reset, a two pole shaper, and an output buffer. The overall chip gain is 16 mV/fC, giving a 50 mV output for a 19,000 electron minimum ionizing particle. The output saturates at 2 volts for a 760,000 electron 'maximum ionizing' input.

The integrator has a folded cascode input, with a 1.6 pF feedback capacitor. When a trigger is received, the switch is opened and integration begins; the measured charge injection during switching is small, and totally masked by noise from the gated grid on the TPC. The integrator maximum charge is more than 2.5 pC, or 800 minimum ionizing particles. The input capacitance is about 10 pF.

The total noise includes contributions from the SAS, SCA and TPC pad. The SAS noise is about 600 electrons plus 13 electrons/pF. The SCA noise is about 1 mV, or about 390 electrons referred to the SAS input. The TPC pads introduce noise because the G-10 insulator is a poor dielectric. The noise is that of a resistor with a $R = \tan(\delta)/\omega C$ where $\tan(\delta)$ is the dielectric loss angle, the fractional energy dissipation per cycle. For our G-10 $\tan(\delta) \sim 0.014$, so the noise is about 300 electrons. Combining these contributions in quadrature gives a total noise of 940 electrons for 15pF pad capacitance, 5% of a minimum ionizing signal. The TPC anode wire gain can be increased if the 20:1 signal to noise ratio proves inadequate.

The chip includes two input protection diodes. While previous TPC electronics[2, 3] have included external protection diodes, our tests indicate that the internal diodes are adequate.

A 200 Ω resistor isolates the diodes from the TPC pads. The omission of external diodes will reduce possible charge buildup on the integrator due to leakage.

The two pole shaper has a 180 nsec FWHM, chosen to match the diffusion time spreading. The FWHM can be varied by about 40an external voltage. A "cold resistor" technique is used to minimize noise. The shaper includes an adjustable 1/t tail correction circuit, to match the measured TPC signal shape for the two gases. The SAS can drive a 50 pF load (2 SCA/ADC chips). The chip also includes internal calibration circuitry. Other specifications include linearity better than 4%, crosstalk less than 0.36%, power consumption of 60 mW/channel, DC output voltage matched within 200 mV for all chips.

The SCA/ADC[5] is identical to that used in CERN NA-49. The 512 sample switched capacitor array can sample up to 40 MHz, with a static and dynamic linearity better than 2% over a 2 volt range, with about 1 mV of noise. We will sample at either 13.8 MHz (P-10) or 6.25 MHz (He–Eth). For the inner TPC rows, we are also considering using different sampling rates for different pseudorapidities, to improve the position resolution at central rapidities.

Because of leakage and charge injection variations, separate pedestals are required for each time bin. Because the measured pedestals will include contributions from the TPC gated grid switching, the SCA clock is generated by the clock/trigger system, and synchronized to the trigger.

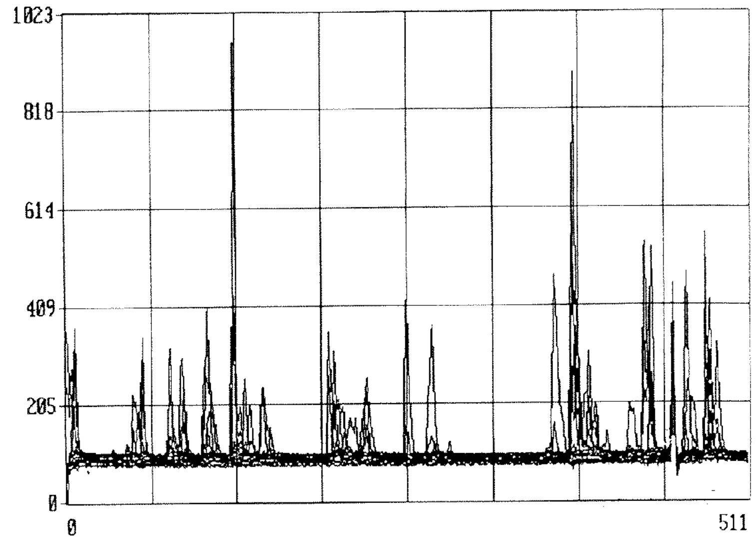

Figure 3. Data taken with strontium 90 source, TPC sector, and FEE card. A minimum ionizing particle would be about 20 ADC counts. Raw data (not pedestal subtacted) from 16 channels are shown superimposed. The signal around time bin 460 where all 16 channels fired is from the ground plane pulser. The overshoot is because the signal has a fast rise time, rather than the TPC-like shape expected by the 1/t tail correction circuit.

The ADC is a 12 bit Wilkinson converter; STAR plans to only use 10 bits of conversion. The converter counts on both edges of a 60 MHz clock. Each channel has its own ADC, so 512 time buckets can be digitized in about 5 msec; because the ADC is double buffered, readout occurs in parallel with the conversion, minimizing deadtime. The chip to chip ADC gain variation is about 20%; we plan to use different resistors to adjust the ramp current to reduce the spread in the system. The overall SCA/ADC power consumption is less than 10 mW/channel.

The electronics is mounted on small (2.9 inch by 7 inch) 32 channel FEE boards, which plug directly into the TPC pad plane, simplifying the cabling. The back of the board includes artwork for two additional SCA's, in case it is ever necessary to double the number of time samples per pad. Pairs of FEE boards are connected to the readout board by a 50 conductor flat ribbon cable.

Data from a FEE board connected to a TPC sector is shown in figure 3. It shows (superimposed) the output from 16 channels, when the TPC is exposed to a strontium-90 source. The wire current draw in the exposed section was about 1 μA. Also visible is a calibration pulse from the TPC ground plane pulser. Because the calibration pulse has a short rise time and no tail, the pulse shows overshoot. For the radioactive pulses, the $1/t$ tail correction circuit removes the tail. The noise measured with this setup is that expected from the SAS, SCA and pad plane dielectric. No additional noise was observed, and rejection of nearby external noise sources was good.

4 DIGITAL CIRCUITRY

Up to 36 FEE boards (1152 TPC pads) can be controlled by a single readout board. The readout board multiplexes the data from the FEE boards over a 1.5 Gbit/sec fiber optic link to the data acquisition system. The readout board also provides trigger, control monitoring and diagnostic functions.

The optical transmitter is a Methode MTM-8510, driven by a HP Gigalink (HDMP-1012) serializer chip. It accepts 20 bits of data at a 60 MHz clock rate - two 10 bit SCA data words in parallel. Transmission is simultaneous with the SCA digitization, so event readout takes a little under 5 msec. The readout control orders the data to optimize the data acquisition system processing speed. The FEE does no data compression; zero suppression is done on the fly by custom ASICs in the DAQ system. The chip also performs bin by bin SCA pedestal subtraction, and channel by channel gain correction.

Figure 4 shows the 40 bit wide, 30 MHz bus that sends data to the serializer. The wide bus necessitates some additional multiplexing, but is necessary because of the speed limits imposed by physical separation between components.

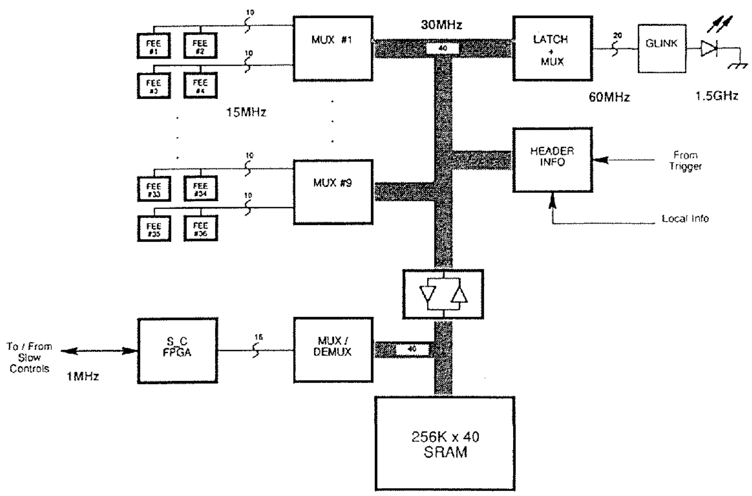

Figure 4. A block diagram of the readout board.

This bus is fed by 9 FPGAs, each of which controls two FEE cables, a total of four FEE boards. The bus also connects to a memory which can store a complete event. The memory can be written to and read from by a slow control link, or by the FEE data stream. This memory and alternate readout path are for diagnostic purposes and use during installation. The controls link can also monitor and adjust voltages on the card, turn groups of four FEE cards on and off and monitor temperatures. It is based on native a 68302 processor serial port, using HDLC protocol running at 1 Mbit/sec. A VME master communicates with the six readout boards of a single supersector over a multi-drop RS-485 link. The slow controls link is mounted on a separate PC board, and has been adopted by other STAR subsystems.

Clock and trigger information is transmitted to the readout boards over a clock and trigger bus. The bus transmits the RHIC strobe, SCA clock and 4 bit wide data nibbles (with clock), the latter at five times the crossing frequency. Each RHIC crossing, the system sends a 4 bit trigger command, a 4 bit DAQ command and a 12 bit trigger token. Trigger commands include triggers, trigger aborts, several calibrations, and a geographical address readout. The DAQ command allows the DAQ and level 3 trigger to respond differently to different types of triggers, such as low multiplicity (two photon) events. The unique 12 bit trigger token ensures that data from different events is not mixed during event building. The trigger bus uses AT&T series 41 differential pECL drivers and receivers, chosen for their high speed and good common mode rejection.

To detect cabling errors, each of the FEE boards and readout boards is tagged with a geographical address. The FEE board addresses are etched into the TPC pad planes; the readout board addresses are encoded in connectors attached to the board mounting. These addresses are read out as a special trigger and passed through the entire event building process, to check that no data is swapped or otherwise confused.

Each readout board receives power over 25 meter long cables from a ± 8 V, 20 A supply. Because of the long cables, regulators are mounted on the readout boards. The supplies themselves are ferro- resonant, chosen for their simplicity, reliability and inherent voltage regulation and overcurrent protection.

5 TESTING AND MONITORING

For a system of this size, testing is a major issue. We have built custom testers for both of the custom IC's and the FEE board. Each tester is composed of a PC, hardware and software (LabWindows) interface, and custom analog circuitry. The SAS tester measures power consumption, gain, noise, crosstalk and signal FWHM in 1 minute per good IC. The SCA tester checks power consumption, gain, noise, in 3 minutes per good IC. We expect yields of about 70% for the SAS and 30% for the SCA, or about 45,000 chips in total. To keep track of the chips individually, each chip is labeled with a bar code; a bar code reader attached to each tester allows quick and accurate entry of the chip number.

The TPC and electronics are monitored by several calibration systems. These include a UV laser which creates ionization tracks, a pulser that pulses the TPC ground plane wires, and the previously described SAS internal calibration circuitry.

6 SYSTEM ISSUES

Because of the size and complexity of STAR, considerable effort has gone into system design. One area of concern was cabling and ground loops; most of the STAR TPC electronics is mounted directly on the detector. All long distance transmission uses optical links or differentially driven cables.

In the FEE, the TPC wheels (support structure) are a single point ground. The power supplies are completely isolated (except for 750 pF/supply capacitative coupling) from ground. The data fibers are, of course, isolated. The clock, trigger and control circuits are all differentially driven to minimize their contribution to ground loops.

Because STAR will use dE/dx below the relativistic rise to help with particle identification, the anode wire gain, and hence temperature must be well controlled, within 0.7°C, so an efficient cooling system is required. The FEE cards have aluminum backers mounted on them behind where the SAS and SCA chips are located. The backers are bolted to an aluminum water cooling channel. Similar channels are bolted to the readout boards. Because of the system size, we have put considerable effort into providing diagnostic and error checking capability, with several calibration systems, an alternate data readout path, and a complete geographical event readout to check the cabling..

Because the large system will be difficult to access, we have made a number of choices to maximize reliability We use ferro-resonant power supplies instead of switching supplies . Each readout board has a bank of 9 individually switchable regulators, so that, for many failures, only a small number of channels will be lost.

7 STATUS

The FEE card design and testing is complete, and the cards have been tested on production TPC sectors The readout board design is complete, with all of the fast logic prototyped on a VME board.

Chip production for the initial build of the electronics is underway, and we expect to complete the initial build next spring, for a cosmic ray test.

8 CONCLUSIONS

We are building a 136,600 channel waveform digitizer system for the STAR TPC, based on two custom IC's. The system requirements have been matched to the TPC parameters: a 20:1 signal to noise ratio for minimum ionizing tracks, 10 bit dynamic range, and 180 nsec FWHM shaping, matched to the TPC diffusion time. The waveform digitizer stores 512 samples at 6.3 or 13.8 MHz, allowing for good single and two track resolution.

The system is highly integrated, with all of the electronics mounted on the detector. All of the analog electronics is mounted in two custom integrated circuits. This integration provides a compact system at an affordable cost.

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