STAR Note # 241

The STAR TPC FEE HDLC Link

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1 Introduction

The STAR TPC requires a slow controls link to the readout boards for a number of monitoring, control and testing tasks. A number of DC voltages and temperatures must be monitored periodically, and the health of the clock and trigger distribution monitored. Event data stored in memory must be able to be read out. The required control tasks include controlling power to groups of FEE cards and programming the SAS chip calibration circuitry. The driving requirement for network speed is that the slow controls network be able to read out TPC data for testing purposes. Since each TPC readout board produces over a megabyte of data per event, we want the link speed to be at least in the 10's of kbytes/sec. This band width must be available over the 30 meters from the platform to the TPC endplates. The link must operate will in the 5kG magnetic field present in STAR; this eliminates standard Ethernet which relies on transformers. Another requirement is that the network be able to be put to sleep during data acquisition if this proves necessary to reduce noise. Finally, the link must accommodate a multi-drop topology to reduce cabling.

To accomplish these tasks, a bi-directional data transmission and control system is required. The link has to interface easily with the EPICS software being used by the STAR slow controls system.. We considered a number of possible links (see Chuck McParland's talk at the Austin HW/SW workshop for details): 1553 (a military standard), BitBus, generic HDLC, Ethernet, IEEE488, LonWorks, JTAG, and serial bus. In November 1994 we chose a link based on generic HDLC (High-level Data Link Control). HDLC is a protocol that supports multi-drop, with some implementations capable of up to 4 Mbits/sec. Examples of large systems built on HDLC include BitBus and LonWorks. Both were rejected for the slow controls link because of the limited bandwidth due to the small packet size imposed by the embedded firmware. The major disadvantage of generic HDLC is that it requires some software development and more on-board hardware than some of the more highly integrated choices.

The link runs reliably at 1 Mbit/sec, with 2024 byte packets providing an effective throughput of 70 kBytes/sec, not counting VME overhead. Each supersector network consists of 6 readout board slave nodes and one commercially built master node based in a VME crate. The slave nodes consist of a 68302 microcontroller (a 68000 core plus communications ports and other enhancements). The link hardware consists of four RS-485 differential pairs, one data and one clock pair in each direction.

2 Hardware

The link nodes are based on a 68302 microcontroller running at 20 MHz, as shown in the block diagram in figure 1. The 68302 bus is A24D16. The system is built on a small (2.9 in by 3.3 in. or 73 mm by 84 mm) PC board which is designed to plug onto a readout board. It can also easily plug onto boards used in other subsystems. The board requires only +5V, at 200mA. It communicates with the readout board by memory mapping. The 68302 address and data lines are brought out to an external connector. Because the 68302 uses a DTACK (data acknowledge) signal, it is possible to connect slow devices such as ADCs directly to the 68302 bus.

The link connection is via four differential pairs. Two pairs carry clock and data from the master to all the slave nodes. One pair is shared by all slaves to send data back to the master. Finally, the clock line is folded back at the slave end of the cable to provide a de-skewed (travel time compensated) receiver clock for the master. The separate pairs for sending and receiving are required by the VME master it only implements RS-422 unidirectional drivers. Unlike BitBus, the 68302 does not support self-clocking. Therefore, the clock signals must be included in the cable.

We currently envision implementing the link with twisted pair cable between the platform and the first readout board, and with flat ribbon cable between the readout boards.

A schematic of the link is given in figure 2. The major components are the 68302, 128 kBytes of PROM and 64 kBytes of static RAM. The system can be reset by an external signal, by command over either serial link, or by cycling the power.

The memory mapping for the on board memory depends on the state of the four chip select lines, according to the following map:

Memory Range	Select Line	Region
000 000 - 00F FFE	CS1	RAM (running)
000 000 - 01F FFE	CS0	prom (startup)
020 000 - 0FF FFE	CS3	Intended for readout board registers
100 000 - 11F FFE	CS0	PROM (running)
400 000 - 40F FFE	CS1	RAM (startup)
700 000 - 70F FFE	none	68302 internal memory, registers
800 000 - FFF FFE	CS2	Intended for readout board event memory.

The on board RAM and PROM only decode address bits A0-A15 and A0-A16 respectively. The higher order bits listed above are mapped into the correct memory by the use of the three chip select lines. This mapping is selectable via eight 68302 internal registers; these mapping registers can be changed. In our implementation, it is changed during the startup procedure; this is why the PROM and RAM appear in different memory locations during startup and normal running.

For testing purposes, we have also designed a mini-motherboard which the link board can plug into. It is shown in figure 3. It contains PROM and RAM sockets, power connections, reset circuitry and a UART. This board is useful for building networks of links, or for testing or prototyping. It also includes eight LEDs which can be controlled by the 68302.

The daughterboard also has a 4 pin RS-232 serial port to which a terminal (or also has a 4 pin RS-232 serial port to which a terminal (or 9600 baud, 8-bit characters, no parity, and one stop bit.

The daughterboard electrical interface is given in the schematic diagrams. The mechanical interface is given in figure 4. Samtec 41 and 51 pin connectors, with a 1mm spacing are used.

3 Network Architecture

The FEE slow controls are divided into 24 separate networks, one for each TPC supersector. Each network has 6 slave nodes, one for each TPC mounted readout board, and a single VME based master, located on the electronics platforms.

For the upcoming system tests, the VME based master will be the Radstone SBCC-1. It is based on a 68360 processor, each board can support four RS-422 HDLC channels. The board costs $2800, or a quite reasonable $700/channel. There are several other boards available with similar capabilities.

The network topology is based on logical and cabling considerations, plus a desire to maximize the network throughput. The individual node addresses are set by 8 bits taken from the motherboard. In the STAR TPC implementation, the addresses are set by the readout board geographical Ids. Each network can in principle contain up to 254 nodes, although driver considerations limit the electrical fanout to about 30 nodes without repeaters.

Within the VME system environment, VxWorks software drivers allow multiple tasks to send and receive messages ("transactions") to various nodes on each network connected to the VME HDLC interface (see above). These drivers allow tasks to issue low level requests (memory reads and writes) as described in figure 5. An appropriate set of EPICS software records will be created to allow EPICS-based control programs to access the HDLC link and perform these same transactions in a transparent manner.

4 Software

Each link node on a network has a unique 8-bit node number. Commands sent via HDLC are usually addressed to a specific node. Some commands may be sent to all nodes simultaneously using the broadcast address 0xff.

Link commands available via HDLC are shown in Figure 5. Figure 6 shows the format of HDLC command and response frames. A C header file is available describing specification codes. A subset of the HDLC command set is available via RS-232. Those commands are shown in Figure 7.

The Reset command causes the 68302 daughterboard hardware and software to undergo the same initialization as occurs at power-on. The link software keeps statistics on the operation of its HDLC and RS-232 communication channels. These statistics – message and error counts – can be read by one command and zeroed by another. The "Fetch node info" command causes the node to return its node number, model number, and the revision number of its PROM software.

Memory access commands permit reading and writing in units of 16-bit words. Commands sent via HDLC may read or write up to 1012 16-bit words. The HDLC command format allows specification of starting address, number of words to read or write, and how many words to skip between words read or written. (A skip value of zero permits a single location to provide or be sent a sequence of values.) Memory access commands entered via RS-232 may read or write just one word at a time.

There are eight general-purpose I/O lines connected to the 68302: four outputs and four inputs. The inputs mat be read, and the outputs set, cleared or read through software one I/O line per command.

Because the data transfer is memory mapped and uses a DTACK signal, timeout can be an issue; it is programmable and can be set up to 800 microseconds, which should be adequate for most ADCs.

5 Status

The link hardware is tested and working well; units are available on loan to other STAR subsystems or other interested parties. The software is at a fairly advanced stage of development. Functional software is available, but it won't be the final version.

6 Conclusions

We have developed a fast (1Mbit/sec) relatively inexpensive data link for the slow controls interface for the STAR TPC electronics. The link hardware and software are at an advanced stage, and we believe that it may be on interest to other STAR subsystems or to other experiments.

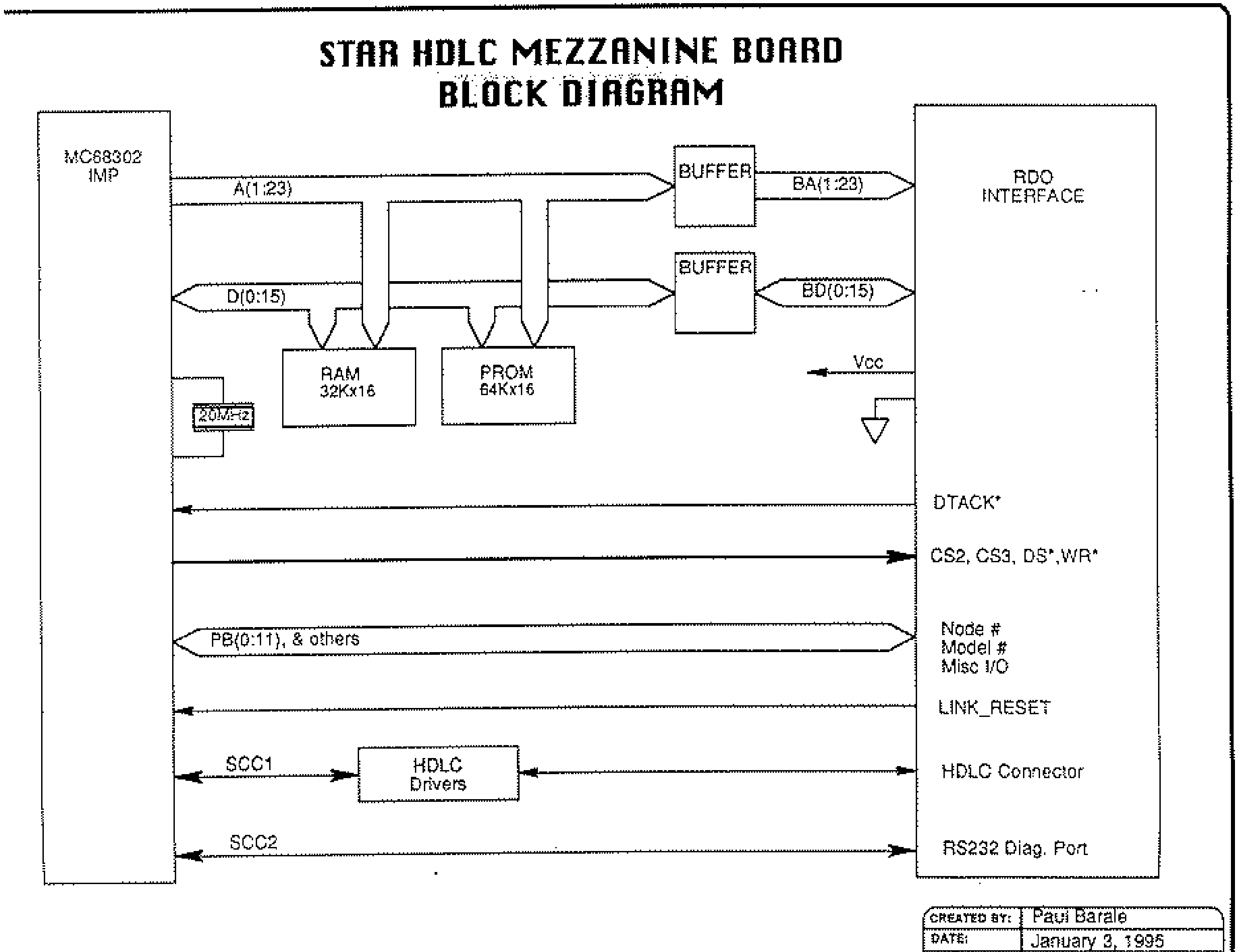

STAR HDLC MEZZANINE BOARD
BLOCK DIAGRAM
MC68302
IMP
A(1:23)
D(0:15)
20MHz
RAM
32Kx16
PROM
64Kx16
BUFFER
BUFFER
BA(1:23)
BD(0:15)
Vcc
RDO
INTERFACE
DTACK*
CS2, CS3, DS*,WR*
PB(0:11), & others
Node #
Model #
Misc I/O
LINK_RESET
SCC1
HDLC
Drivers
HDLC Connector
SCC2
RS232 Diag. Port
CREATED BY: Paul Barale
DATE: January 3, 1995
UPDATED BY: Fred Bieser
UPDATED: June 22, 1995

Figure 1.

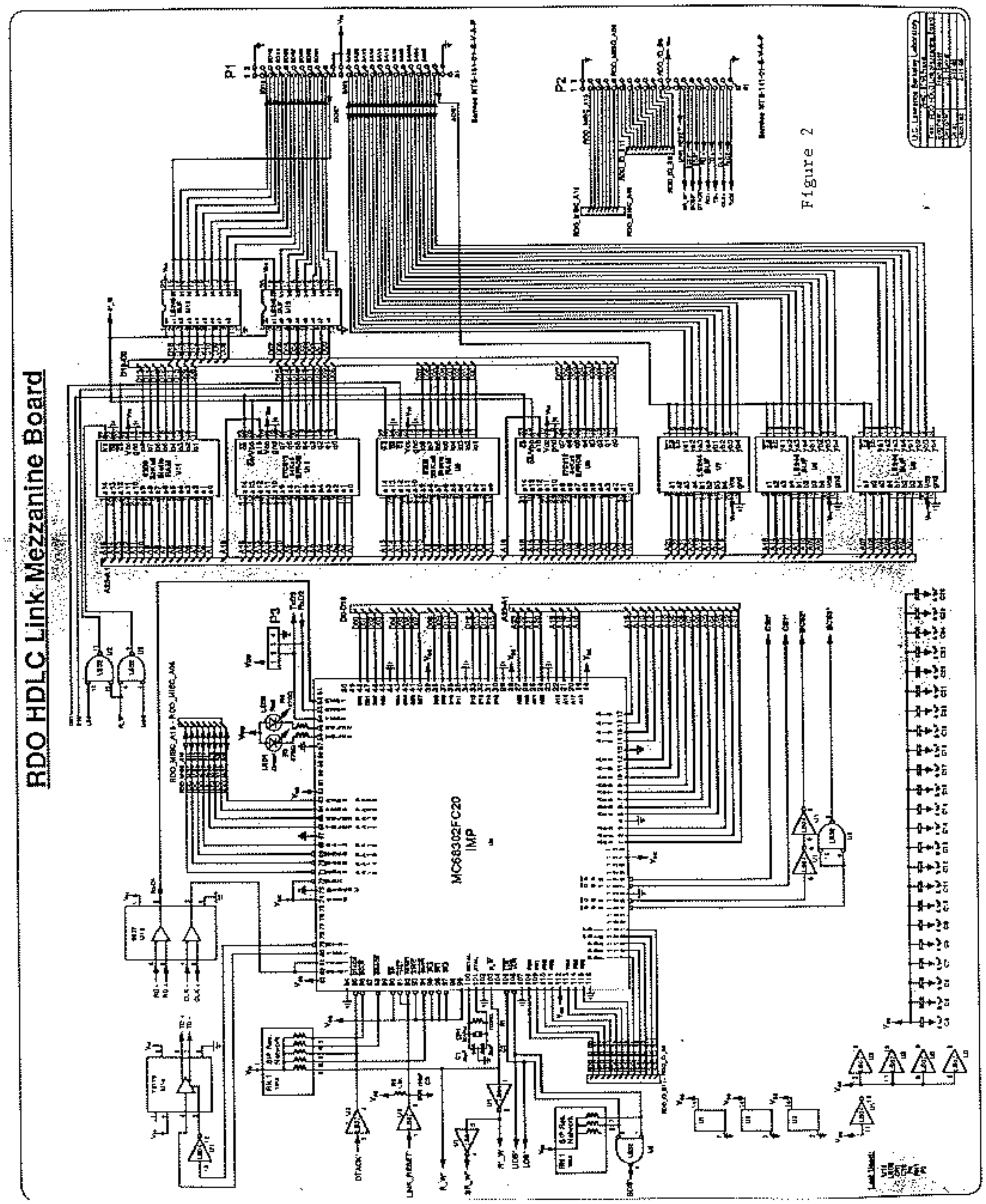


Figure 2

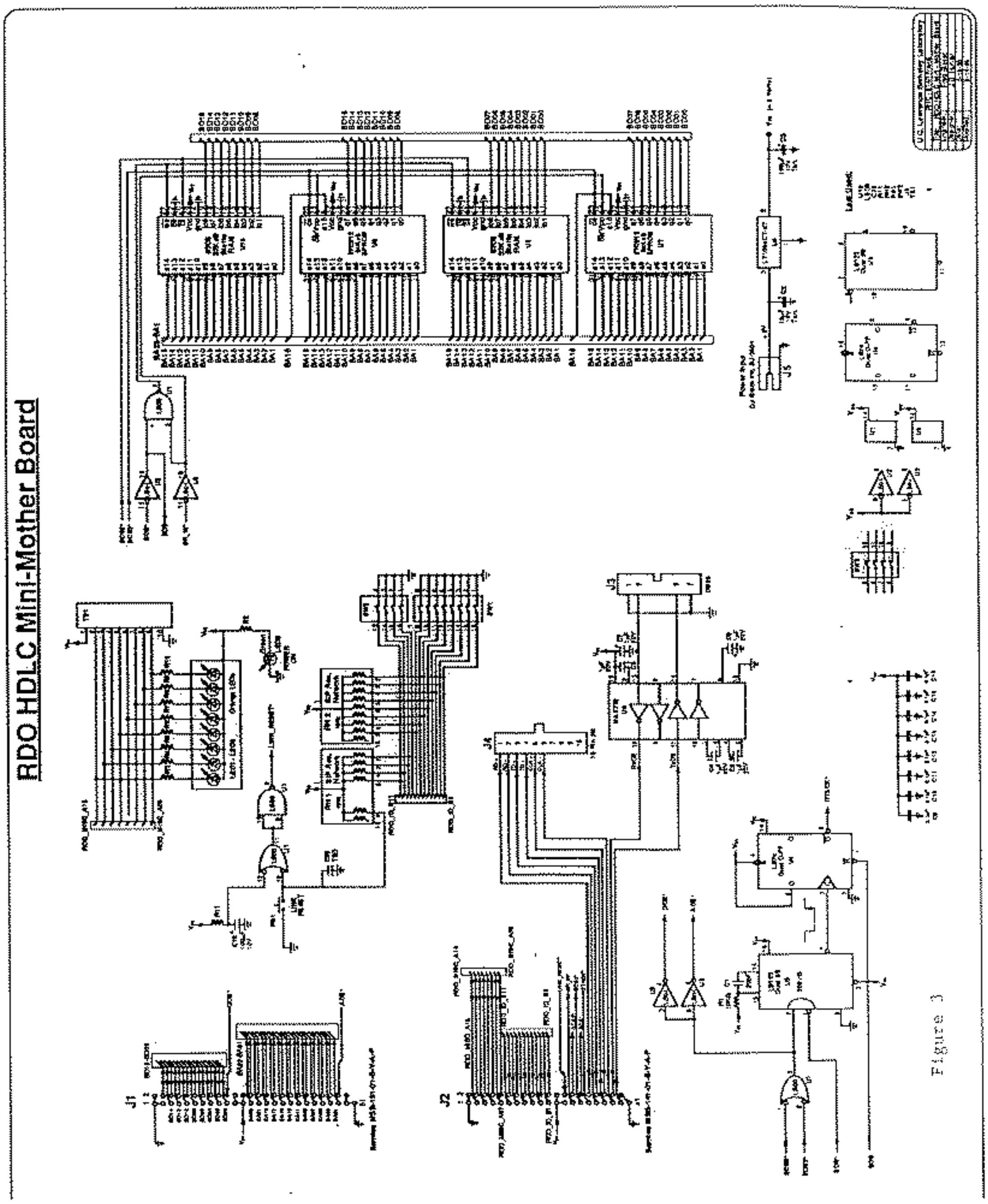
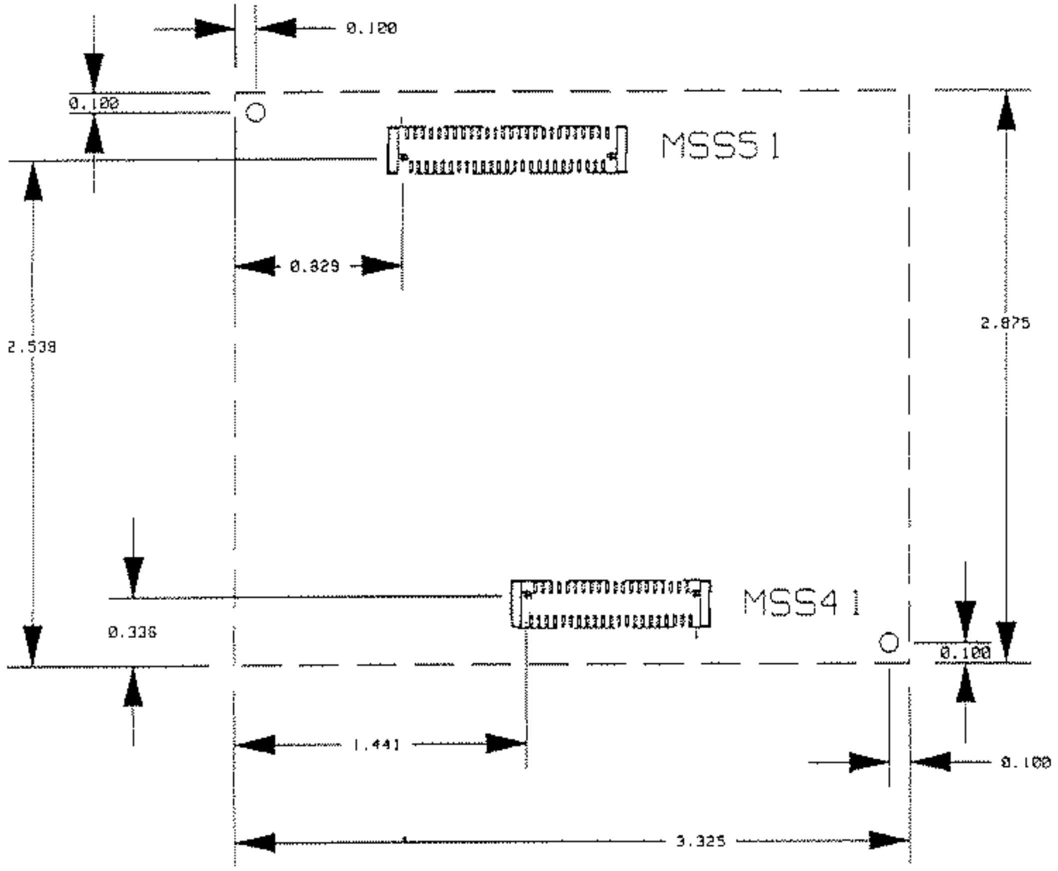


Figure 3

Figure 4

STAR HDLC Mezzanine Board



All Dimensions are in Inches

Command	**Command Code**	**Notes**
Reset 68302	01	1.
Clear node statistics	02	1.
Fetch node statistics	03	
Fetch node information	04	2.
Read privileged memory block	05	
Write privileged memory block	06	
Read unprotected memory block	07	
Write unprotected memory block	08	
Write unprotected block, do not respond	0c	1.
Set output bit	09	
Clear output bit	0a	
Read input or output bit	0b	

Notes:

1. May be braodcast to all nodes; no response frame returned.

2. May be sent to broadcast address. Projected use is to query node when its node number is in doubt.

Figure 5. Link Commands Available via HDLC.

Command Frame Format

Byte Address (hex)	
00	Recipient's node number | (unused)
02	Message ID - upper word
03	Message ID - lower word
06	Length of this frame (exclusive of CRC)
08	Command function code
0a	Bit specification for bit set/clear/read commands
0a	Memory address - upper word
0c	Memory address - lower word
0e	Word count - upper word
10	Word count - lower word
12	Word offset - upper word
14	Word offset - lower word
16	Data to be written - first word
18	.
.	.
.	.
.	.

Response Frame Format

Byte Address (hex)	
00	Responder's node number | (unused)
02	same Message ID as in command frame
04	Message ID - lower word
06	Length of this frame (exclusive of CRC)
08	Response status code
08	Value of bit read
0a	Data read or statistics requested
.	.
.	.
.	.

Figure 6. HDLC Link Command and Response Frame Formats

?	Print this message
H	Help - print this message

addr	Display [and modify] 16-bit memory location.
	Enter hexadecimal address to see mem location data.
	    address
	To modify, enter hex value on same line as data
	For example, to put 0x6000 in location 0x700006
	    : 700006
	    0834 6000

RI	Read Input bit (1, 2, 3, or 4) **RI** *bit*
RO	Read Output bit (1, 2, 3, or 4) **RO** *bit*
S	Set output bit (1, 2, 3, or 4) **S***bit*
Z	Zero (clear) output bit (1, 2, 3, or 4) **Z** *bit*
GI	Get node infor (node #, model #, PROM version)
GS	Get all node statistics
GSH	Get HDLC statistics only
GSU	Get UART statistics only
ZS	Zero (clear) node statistics
RESET	Reset 68302 CPU

Figure 7. Link Commands Available via RS-232