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ALICE DETECTOR DATA LINK

ALICE-DDL

Hardware Guide for the Front-end Designers

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1 Document information

1.1 Abstract

This document describes the standard interface between the DDL Source Interface Unit and the Front-end Electronics of the ALICE sub-detectors in detail. It is based on the Interface Control Document [1].

1.2 Document status sheet

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3. Issue	**4. Revision**	**5. Data**	**6. Reason for change**
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Final	1.3	24 January, 2001	new *4.2 JTAG interface description* sub-chapter
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Table 1 Document Status Sheet

1.3 Document change record

Document Change Record			**DCR No.**	
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Table 2 Document Change Record (of changes made since issue ...)

1.4 Table of contents

1.5 List of figures

1.6 List of tables

2 Introduction

2.1 Purpose of the document

This document has been written for the FEE designers to provide all the necessary information for the design and the test of the FEE-SIU interface. It shall be used together with the ICD [1], which contains the basic information on the DDL interfaces.

2.2 Scope

2.2.1 Concept

All the ALICE sub-detectors will be connected to the DAQ though a standard detector read-out chain, consisting of the DDL and the RORC. The main task of the DDL is to transmit event data from the FEE to the RORC. The DDL is however, a multi-purpose link that can also be used as a medium for the remote control and test of the FEE from the DAQ. For these purposes, the DDL shall be able to transmit: commands from the DAQ to the FEE, status words in the opposite direction and data blocks in both directions, according to the standard protocol. The DDL consists of three main parts: the SIU, the DIU and the physical medium. The RORC can act as:

- input buffer of the event data, transmitted from the FEE;
- output buffer for detector control data blocks, transmitted to the FEE;
- interface between the FEDC and the DDL for sending commands and receiving status words.

The DDL transfers event fragments from the experimental pit to the computing room and stores them in the input buffer of the RORC. The FEDC is responsible for the sub-event building. The LDC reads-out the event fragments from the RORCs and assembling them into sub-events. Then the sub-events are sent to the central event building switch. Figure 1 shows the concept of the detector read-out chain.

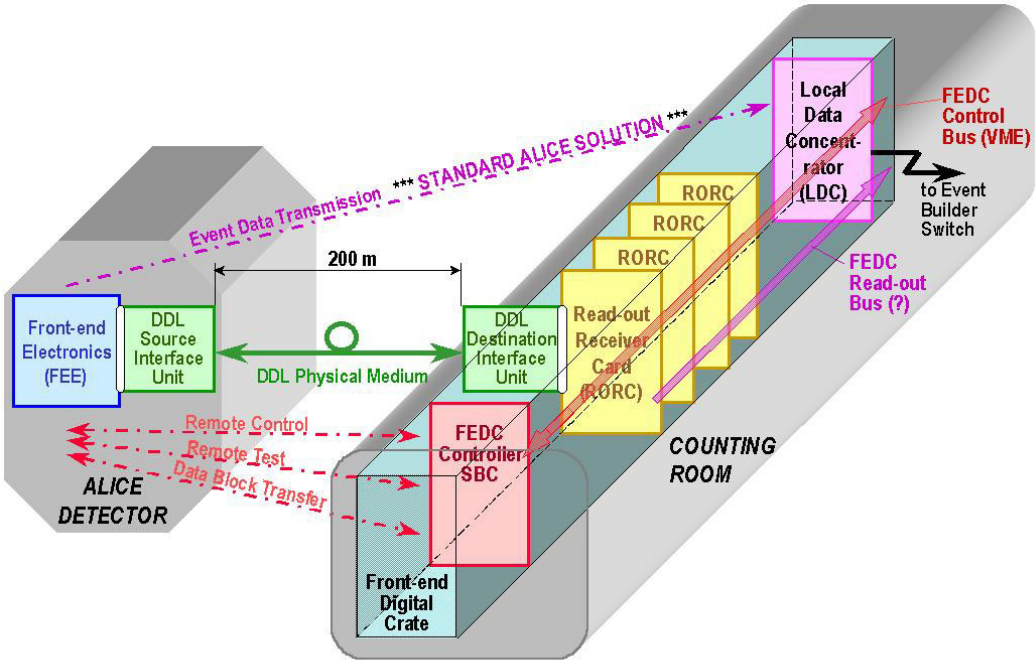


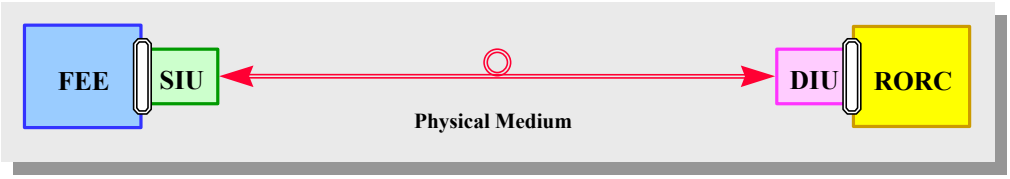
Figure 1 The concept of the detector read-out chain

2.2.2 DDL Configurations

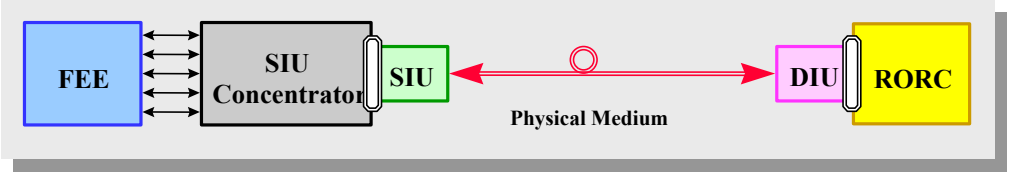
The DDL can be used in three different configurations:

- SIU-DIU configuration (see Figure 2/a)
- SIU-DIU configuration with SIU concentrator (see Figure 2/b)
- DIU-DIU configuration (see Figure 2/c).

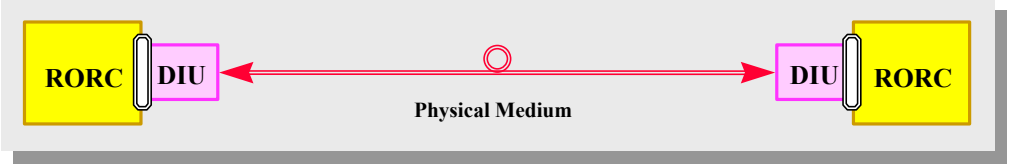
In DAQ point view these configurations are identical, so the DAQ can execute all the transactions, according to the standard DDL protocol.



a.) SIU - DIU configuration



b.) SIU - DIU configuration with SIU concentrator



c.) DIU - DIU configuration

Figure 2 The different DDL configurations

In *SIU-DIU configuration* a SIU, a DIU and a RORC are used. The SIU is connected to the FEE and placed inside the detector. The DIU is connected to the RORC and they are located in the counting room. These subsystems are controlled by the DDL control software, running on the LDC. Apart from the DDL's physical medium, no other cabling will be used for the information transfer between the DAQ and the devices connected to the far end of the DDL (FEE and SIU). This configuration is recommended for most of the ALICE sub-detectors.

The *SIU-DIU configuration with SIU concentrator* is similar to the SIU-DIU configuration, however the SIU is placed outside of the detector and it is connected to a so called SIU concentrator board. The information is transferred between the FEE and the SIU concentrator through medium speed (electrical) links for a distance of 2-10 meters. This configuration is foreseen for the Pixel detector, where the level of the radiation will be too high for the SIU.

In *DIU-DIU configuration* the information are transmitted between two VME crates. In this case two DIUs and two RORCs are used. The *Master* RORC and its DIU are located in the counting room at the DAQ side of the DDL and they are controlled by the DDL control software. The *Slave* RORC and its DIU are located in the pit at the detector side of the DDL and they are controlled by the FEE/SIU emulator software. In DDL protocol point of view, the *Slave* RORC plays the role of the FEE, while its DIU the role of the SIU. This configuration is foreseen for the trigger detectors.

2.2.3 Connection of the SIU to the FEE

The SIU is connected to the FEE via the FEE-SIU interface [1] and a TAP [2]. All the FEEs shall implement the FEE-SIU interface and it can be used for the event data transmission and also for the control and test of the FEE. The front-end buses of the FEEs are controlled by the SIU through the FEE-SIU interface. The different ALICE sub-detectors will have different mechanical and electrical parameters and they will run at different clock frequencies. Thus no common technical solution is possible for the architecture, the transceivers and the termination of the front-end buses. The design consideration for FEE motherboard layout is presented in this document (see chapter 4.1), **but the FEE designers shall take the responsibility for the complete design of the front-end bus.**

The implementation of the TAP is optional. It can only be used for the control and test of the FEE. **The complete JTAG circuitry of the FEE board shall be designed by the FEE designers.** The frequency of the *TCK* signal (provided by the SIU) is not fixed, so the front-end designers have a freedom to choose among different values.

2.3 Acronyms

DAQ	Data Acquisition System
DDL	ALICE Detector Data Link
DIU	DDL Destination Interface Unit
FEE	Front-end Electronics
FEDC	Front-end Digital Crate
HG	Hardware Guide for the Front-end Designers
ICD	Interface Control Document
LDC	Local Data Concentrator
PhI	Physical and Signalling Interface Specification
RORC	Read-out Receiver Card
SIU	DDL Source Interface Unit
TAP	Test Access Port

2.4 Abbreviations

DTSTW	Data Transmission Status Word (*Interface Command*)
EOB	End of Data Block (*Front-end Status Bit*)
EOBTR	Close any Block Transmission Transaction (*Front-end Command*)
FECMD	Front-end Command
FECTRL#address	Front-end Control (*Front-end Command*)
FESTRD#address	Front-end Status Read-out (*Front-end Command*)
FESTW	Front-end Status Word
RDYRX	Open an Event Data Transmission Transaction (*Front-end Command*)
SRTS	SIU Reset (*Interface Command*)
STBRD#address	Open a Data Block Read Transaction (*Front-end Command*)
STBWR#address	Open a Data Block Write Transaction (*Front-end command*)

2.5 References

[1] Interface Control Document, ALICE/96-43, Internal Note/DAQ, 12 December 1996
[2] IEEE Standard Test Access Port and Boundary Scan Architecture, IEEE Std 1149.1-1990 and IEEE Std 1149.1a-1993

2.6 Overview of the document

The first chapter of this document contains:

1. the abstract
2. the document status sheet
3. the document change record
4. the table of contents
5. the list of figures
6. the list of tables

The second chapter of this document contains:

1. the purpose of the document
2. the scope
3. the acronyms
4. the abbreviations
5. the references
6. an overview of the document

The third chapter of this document describes:

1. the physical description
2. the electrical description
3. the FEE-SIU interface signals
4. the signal functions of the TAP
5. the pin assignment of the interface connector
6. the front-end commands
7. the front-end status words
8. the interface timing

The fourth chapter of this document contains:

1. the drawing of the SIU board
2. the suggested PCB layout on the FEE motherboard
3. the preliminary specification of the JTAG interface

3 General description

3.1 Physical description

The SIU card has a physical arrangement as it shown in Figure 3. There are three connectors on the SIU board: the two interface connectors and the physical medium connector. Two CMC format 64-pin connectors[1] are used as interface connectors. They connect the SIU to the motherboard of the FEE, containing all the signals of the FEE-SIU interface, the TAP and also the power and the ground lines. The plugs[2] are mounted on the SIU and the receptacles[3] on the FEE. A duplex fibre optic connector is used for the connection of the SIU card to the physical medium. The receptacle of this connector is mounted on this card, while the plug on the optical fibres. The precise position of the plug interface connectors and the standoffs is shown in the Figure 3.

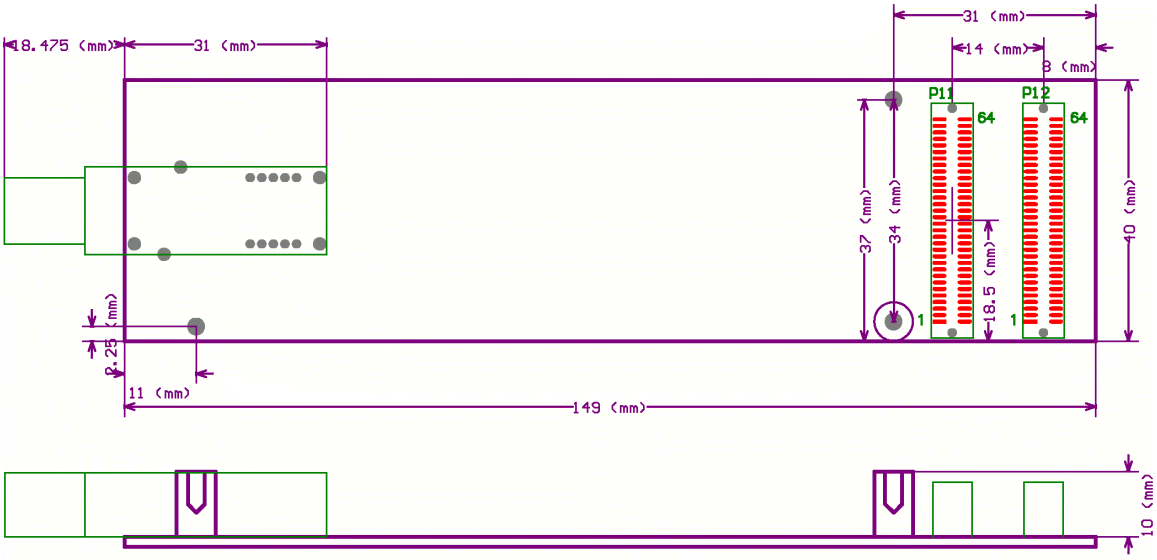


Figure 3 The physical arrangement of the SIU card

[1] IEEE, "Common Mezzanine Format (CMC)", IEEE-1386.
[2] Tyco Electronics (AMP) – 120527-1
[3] Tyco Electronics (AMP) – 120521-1

3.2 Electrical description

3.2.1 Power requirement

The SIU will operate from a single +3.3V power supplies. It shall be supplied from the FEE through the interface connector (see). The maximum power consumption of the SIU will be less than 5 W.

3.2.2 Signal levels

The FEE-SIU interface lines and the TAP lines are connected to the I/O pins of the SIU protocol chip. The V_{CCIO} pins of this IC are connected to the +3.3V power supply. The output high is compatible with either the +3.3 V or the +5 V systems. The inputs of the protocol chip are NOT+5V tolerant, so only +3.3 V power supplies can be used for the drivers and the receivers of the front-end bus and the TAP on FEE motherboard. Table 3 shows the signal levels of the FEE-SIU interface and the TAP.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	high-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		-0.5	0.8	V
V_{OH}	high-level LVTTL output voltage	I_{OH}[4] = -12 mA DC	2.4		V
	high-level CMOS output voltage	I_{OH}[5] = -0.1 mA DC	3.1		V
V_{OL}	Low-level LVTTL output voltage	I_{OL}[6] = 12 mA DC		0.4	V
	Low-level CMOS output voltage	I_{OL}[7] = 0.1 mA DC		0.2	V
I_I	input leakage current	V_I[8] = 4.1V to –0.5V	-10	10	µA
I_{OZ}	tri-state output off-state current	V_O[9] = 4.1V to –0.5V	-10	10	µA

Table 3 The signal levels of the FEE-SIU interface and the TAP

[4] High-level output current
[5] High-level output current
[6] Low-level output current
[7] Low-level output current
[8] Input voltage
[9] Output voltage

3.3 FEE-SIU interface signals

3.3.1 Signal name conventions

All the signal names of the DDL interfaces are composed of four components: the interface identifier, the direction identifier, name identifier and the polarity identifier.

The DDL has two interfaces: the FEE-SIU interface and the RORC-DIU interface. The signals which belong to the FEE-SIU interface are prefixed with a letter "**f**".
The direction of the signals are defined from the point of view of the external systems (e.g. FEE, RORC). The input signals are indicated with an abbreviation "**i**", the output signals with "**o**", while the bi-directional signals with "**b**". In the signal name the direction identifier follows the interface identifier.
The name identifier is the abbreviation of the natural name of the signal. It shall be written by uppercase letters (e.g. DATA[31..0] -> **D[31..0]**, CONTROL -> **CTRL**). In the signal name the name identifier follows the direction identifier. Figure 4 shows all of the interface signals with their natural names and signal names.
The polarity identifier indicates the polarity of the active state of the signal. This identifier are "**_N**" characters for the active low signals and it is nothing for the active high signal. In the signal name the polarity identifier is located at the end.

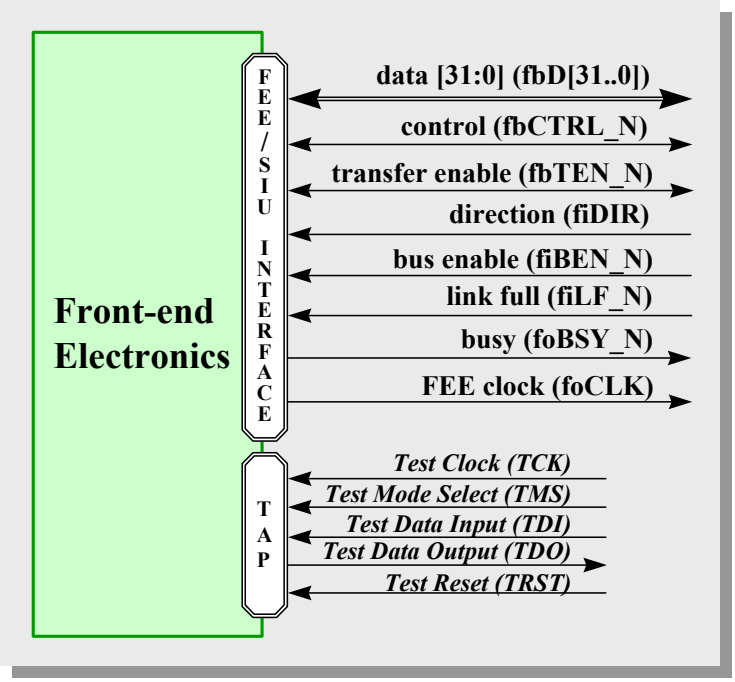


Figure 4 The names of the SIU-FEE interface and the TAP signals

3.3.2 Signal line functions

All of the signals of the FEE-SIU interface are synchronised to the foCLK signal.

fbD[31..0]	**DATA[31..0]**	**bi-directional**	

The fbD[31..0] is a 32 bit wide, tri-state data bus. If the level of the fiDIR line is high, the data on these bus lines are transferred from the FEE to the SIU on a low-to-high transition of the foCLK when the fbTEN_N is active. The fbD[31..0] contains status words when the fbCTRL_N is active, otherwise it contains normal data words. If the level of the fiDIR line is low, the data on these bus lines are transferred from the SIU to the FEE on a low-to-high transition of the foCLK, when the fbTEN_N is active. The fbD[31..0] contains commands, when the fbCTRL_N is active, otherwise it contains normal data words.

fbCTRL_N	**CONTROL**	**bi-directional**	**active low**

The fbCTRL_N is a tri-state management line for the data bus. The active level of this line indicates that the data word to be transferred between the FEE and the SIU is a command or a status word, depending on the direction of the information transfer. It is a status word, when the information is transferred from the FEE to the SIU, otherwise it is a command.

fbTEN_N	**TRANSFER ENABLE**	**bi-directional**	**active low**

The fbTEN_N is a tri-state management line for the data bus. The active level of this line enables data to be transferred between the FEE and the SIU on the low-to-high transition of the foCLK. The direction of the information transfer depends on the level of the fiDIR line.

fiDIR	**DIRECTION**	**input**	**high: FEE to SIU transfer**

The fiDIR is a management line for the data bus. The high level of this line indicates that the information is transferred from the FEE to the SIU on the fbD[31..0] lines, while the low level indicates the opposite direction of the information transfer. When the level of this line is high, all of the bi-directional lines are driven by the FEE, otherwise they are driven by the SIU.

fiBEN_N	**BUS ENABLE**	**input**	**active low**

The fiBEN is a management line for the data bus. The inactive level of this line will put in high-impedance state the tri-state drivers of all the bi-directional lines of the FEE-SIU interface in the SIU and in the FEE.

fiLF_N	**LINK FULL**	**input**	**active low**

The fiLF_N is a flow control line. The active level of this line indicates that the FEE shall stop the data block transfer and the FESTW(EOB=1) status word transfer to the SIU, because the SIU and/or the DIU and/or the RORC are busy. After this line becomes active, only one more data word or status word may be transferred from the FEE to the SIU.

foBSY_N	**BUSY**	**output**	**active low**

The foBSY_N is a flow control line. The active level of this line indicates that the FEE is not able to receive data block from the DDL. After this line become active, only one more data word may be transferred from the SIU to the FEE.

foCLK	**FEE CLOCK**	**output**	

The foCLK is a clock line. This free running clock is generated by the FEE for the synchronisation of the information transfer between the FEE and the SIU.

3.4 Signal line functions of the TAP

1. The **TCK** provides the clock for the test logic.
2. The signal received at **TMS** is decoded by the TAP controller to control the test operations.
3. Serial test instructions and data are received by the test logic at **TDI**.
4. The **TDO** is the serial output for test instructions and data from the test logic.
5. The **TRST** provides for asynchronous initialisation of the TAP controller.

3.5 Pin assignment of the interface connector

Two 64-pin connectors are used for the SIU-FEE interface and for the TAP as well. The pin assignment of these connectors can be seen in Table 4.

CMC SIU (P11 connector)			
1	FIBEN_N	-12V	2
3	GND	FILF_N	4
5	FOBSY_N	FIDIR	6
7	BUSMODE1#	+5V	8
9	FBCTRL_N	FBTEN_N	10
11	GND	FBD0	12
13	FOCLK	GND	14
15	GND	FBD1	16
17	FBD2	+5V	18
19	V(I/O) (+3.3V)	FBD3	20
21	FBD4	FBD5	22
23	FBD6	GND	24
25	GND	FBD7	26
27	FBD8	FBD9	28
29	FBD10	+5V	30
31	V(I/O) (+3.3V)	FBD11	32
33	FBD12	GND	34
35	GND	FBD13	36
37	FBD14	+5V	38
39	GND	FBD15	40
41	FBD16	FBD17	42
43	FBD18	GND	44
45	V(I/O) (+3.3V)	FBD19	46
47	FBD20	FBD21	48
49	FBD22	+5V	50
51	GND	FBD23	52
53	FBD24	FBD25	54
55	FBD26	GND	56
57	V(I/O) (+3.3V)	FBD27	58
59	FBD28	FBD29	60
61	FBD30	+5V	62
63	GND	FBD31	64

CMC SIU (P12 connector)			
1	+12V (1)	TAP_TMS	2
3	TAP_TDI	TAP_TDO	4
5	TAP_TCK	GND	6
7	GND	TAP_TRST	8
9	-	-	10
11	BUSMODE2#	+3.3V	12
13	-	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	-	GND	18
19	-	-	20
21	GND	-	22
23	-	+3.3V	24
25	-	-	26
27	+3.3V	-	28
29	-	GND	30
31	-	-	32
33	GND	-	34
35	-	+3.3V	36
37	GND	-	38
39	-	GND	40
41	+3.3V	-	42
43	-	GND	44
45	-	-	46
47	GND	-	48
49	-	+3.3V	50
51	-	-	52
53	+3.3V	-	54
55	-	GND	56
57	-	-	58
59	GND	-	60
61	-	+3.3V	62
63	GND	-	64

Table 4 The pin assignment of the FEE-SIU interface connectors

3.6 Front-end commands

The FECMDs are send from the RORC to the FEE through the DDL. There are only two standard FECMDs that shall be implemented and used by the FEEs of each sub-detector:

Ready to Receive (RDYRX);
End of Block Transfer (EOBTR).

An event data transmission transaction can be opened by using a RDYRX command. The RORC may only send this command to the FEE through the DDL, when it is ready to receive event data. When the FEE receives this command, it shall transfer an event data block to the SIU after receiving a L2-accept signal from the trigger system.

Any open block transfer transactions (e.g. event data transmission, user defined block write/read) shall be closed by the FEE, when it receives an EOBTR command.

The implementation and application of the following 4 user defined FECMDs is optional:

Start of Block Write (STBWR#address);
Start of Block Read (STBRD#address);
Front-end Control (FECTRL#address);
Front-end Status Read-out (FESTRD#address).

A *block write* transaction can be opened by using a STBWR command. In this transaction a data block will be downloaded from the RORC to the FEE at the *address* defined in the parameter field of the STBWR command.

A *block read* transaction can be opened by using a STBRD command. In this transaction a data block will be read by the RORC from the FEE at the *address* defined in the parameter field of the STBRD command.

The STBWR and the STBRD commands can be used only, if the memories of the FEE are organised as memory banks. This organisation allows to read and write data blocks sequentially word-by-word from/to a given starting address of the FEE memories, without generating address cycle on the front-end bus.

The FEE can be controlled by using FECTRL commands. Each *address* can represent an independent control function.

Status words can be read-out from the FEE by using FESTRD commands. Each *address* can represent an independent status word read-out function.

D31	D30 D12	D11 D8	D7	D6	D5	D4	D3	D2	D1	D0	data bits
	PARAMETER FIELD	IDENTIFIER FIELD	CODE FIELD				DESTINATION FIELD				command fields
X	FEE address	transaction ID	WRITE	UD	CLOSE	BTR	reserved	FEE	SIU	DIU	FECMD
X	is not used	transaction ID	0	0	0	1	0	1	0	0	RDYRX
X	is not used	transaction ID	1	0	1	1	0	1	0	0	EOBTR
X	address in FEE	transaction ID	1	1	0	1	0	1	0	0	STBWR#address
X	address in FEE	transaction ID	0	1	0	1	0	1	0	0	STBRD#address
X	address in FEE	transaction ID	1	1	0	0	0	1	0	0	FECTRL#address
X	address in FEE	transaction ID	0	1	0	0	0	1	0	0	FESTRD#address

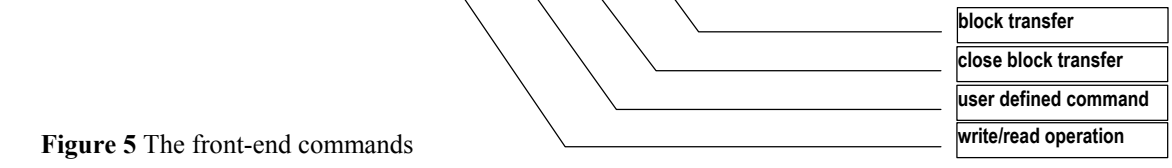


Figure 5 The front-end commands

3.7 Front-end status words

There are two different types of the FESTWs:

1. The RORC can read-out a FESTW(EOB=0) status word by sending a FESTRD#address command. These sub-detector specific status words shall be defined by the FEE designers. The parameter field is reserved for FEE specific status information, while the error bit can be used for the indication of any predefined error states inside the FEE.
2. A FESTW(EOB=1) status word shall automatically be generated by the FEE, when the transfer of an event or data block from the FEE to the SIU is terminated. In this case the parameter filed may contain the length of the transmitted event or data block, but this is not mandatory. The error bit shall be set to '1' if any errors have been detected inside the FEE during the data block transfer.

In the identifier field of any FESTWs, the FEE shall always return the ID number of the current transaction.

D31	D30 D12	D11 D8	D7	D6	D5	D4	D3	D2	D1	D0
ERROR BIT	PARAMETER FIELD	IDENTIFIER FIELD	CODE FIELD				SOURCE FIELD			
error/OK	status parameter	transaction ID	status code		EOB	reserved	reserved	FEE	SIU	DIU
error	front-end status	transaction ID	0	1	0	0	0	1	0	0
error	data block length	transaction ID	0	1	1	0	0	1	0	0

at the end of an event or a data block

in the front-end status read-out transaction

Figure 6 The front-end status words

Receiving a FESTW(EOB=1) status word, the SIU shall generate a DTSTW (see Figure 7) and send it to the RORC. The different fields of the DTSTW shall be processed by the SIU, according to the following rules:

- The *error bit* received in the FESTW, shall be retransmitted.
- The number of the received data words in an event or in a data block, shall be counted for the identification of the *block length*.
- The *transaction ID* received in the FESTW, shall be retransmitted.
- A new *code field* shall be generated.
- A new *source field* shall be generated.

D31	D30 D12	D11 D8	D7	D6	D5	D4	D3	D2	D1	D0
ERROR BIT	PARAMETER FIELD	IDENTIFIER FIELD	CODE FIELD				SOURCE FIELD			
error	data block length	transaction ID	1	0	0	0	0	0	1	0

Figure 7 The data transmission status word

3.8 Interface timing

3.8.1 AC characteristics of the FEE-SIU interface signals

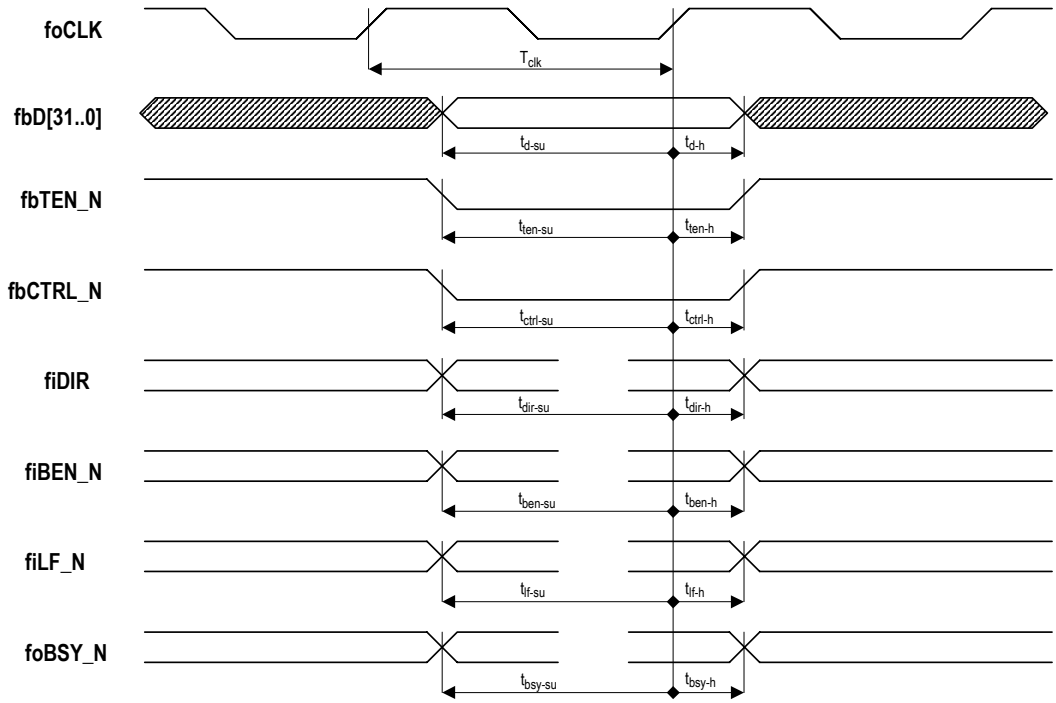


Figure 8 Timing waveforms of the FEE-SIU interface signals

Symbol	Parameter	Unit	Min.	Max.
T_{clk}	foCLK clock period	ns	15	-
T_{sym}	clock symmetry (duty cycle)	%	40	60
t_{d-su}	fbD[31..0] setup time	ns	8	-
t_{d-h}	fbD[31..0] hold time	ns	0	-
t_{ten-su}	fbTEN_N setup time	ns	8	-
t_{ten-h}	fbTEN_N hold time	ns	0	-
$t_{ctrl-su}$	fbCTRL_N setup time	ns	8	-
t_{ctrl-h}	fbCTRL_N hold time	ns	0	-
t_{dir-su}	fiDIR setup time	ns	8	-
t_{dir-h}	fiDIR hold time	ns	0	-
t_{ben-su}	fiBEN_N setup time	ns	8	-
t_{ben-h}	fiBEN_N hold time	ns	0	-
t_{lf-su}	fiLF_N setup time	ns	8	-
t_{lf-h}	fiLF_N hold time	ns	0	-
t_{bsy-su}	foBSY_N setup time	ns	10	-
t_{bsy-h}	foBSY_N hold time	ns	0	-

Table 5 AC characteristics of the FEE-SIU interface signals

3.8.2 SIU reset

The SIU reset cycle can be started by the RORC, transmitting a SRST interface command to the SIU. When the SIU receives the SRST command, it activates the fiBEN_N interface line and put in inactive state the fbCTRL_N, the fbTEN_N and the fbLF_N interface lines. The SIU sets the fiDIR interface line in logical '0' level, so the front-end bus is directed from the SIU towards the FEE. The SIU reset cycle will be automatically started after each power on as well.

3.8.3 Basic data, command and status transfer between the FEE and the SIU

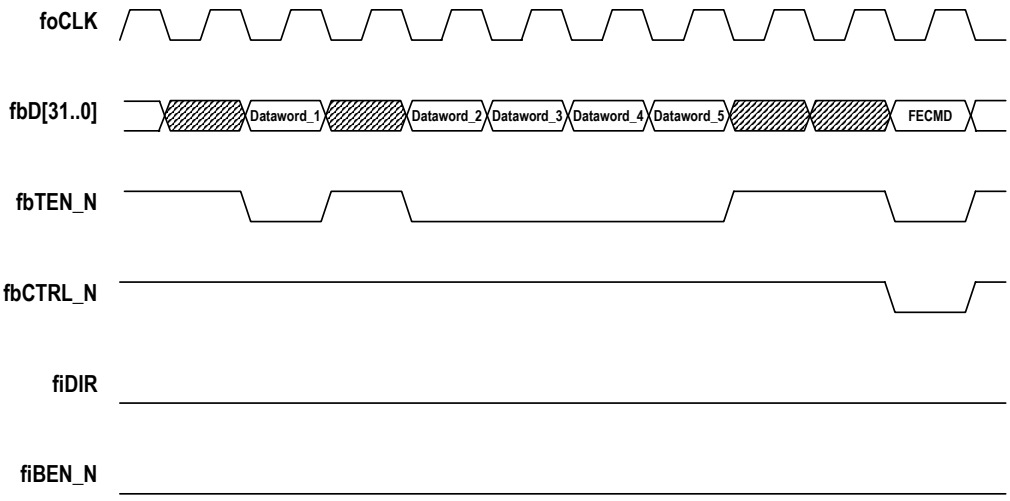


Figure 9 Data and command transfer from the SIU to the FEE

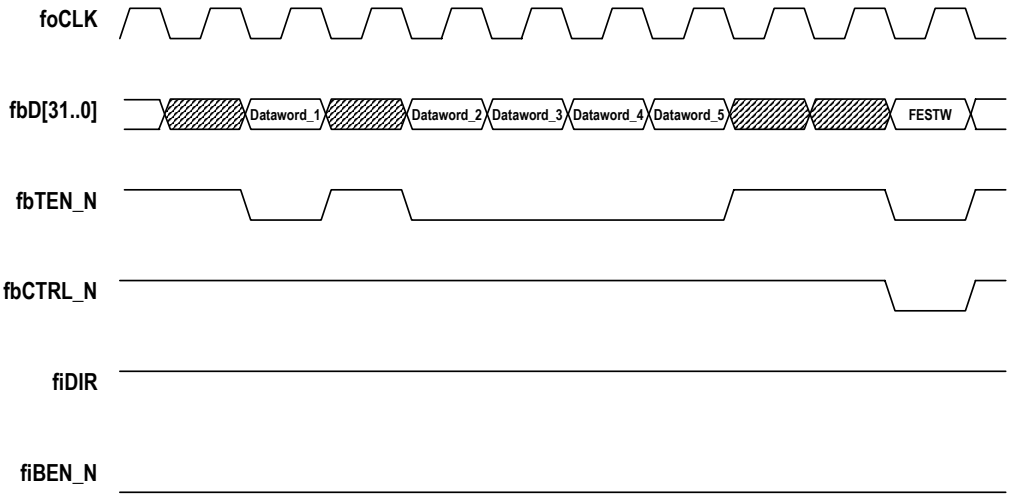


Figure 10 Data and status word transfer from the FEE to the SIU

3.8.4 Front-end status read-out transaction

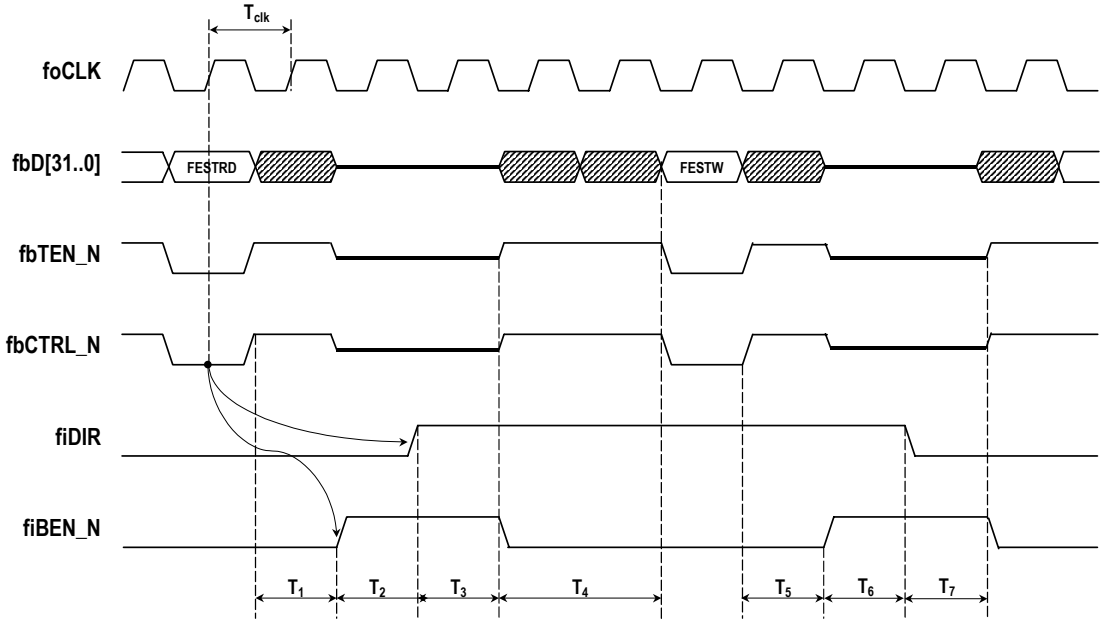


Figure 11 The front-end status read-out transaction

Symbol	Parameter	Unit	Min.	Max.
T_{clk}	foCLK clock period	ns	15	-
T_1	the SIU shall put the front-end bus in off-state after a FESTRD command has been transferred from the SIU to the FEE	T_{clk}	1	1
T_2	the SIU shall change the direction of the front-end bus after the front-end bus has been put in off-state	T_{clk}	2	2
T_3	the SIU shall put the front-end bus in on-state after the direction of the front-end bus has been changed	T_{clk}	2	2
T_4	the FEE shall assert the FESTW on the front-end bus after the front-end bus has been put in on-state	T_{clk}	1	4[10]
T_5	the SIU shall put the front-end bus in off-state after a FESTW has been transferred from the FEE to the SIU	T_{clk}	1	1
T_6	the SIU shall change the direction of the front-end bus after the front-end bus has been put in off-state	T_{clk}	2	2
T_7	the SIU shall put the front-end bus in on-state after the direction of the front-end bus has been changed	T_{clk}	2	2

Table 6 The front-end status read-out timing requirements

[10] The front-end time-out bit in the SIU status register will be set to '1', if the FEE do not assert the FESTW on the front-end bus within the defined period.

3.8.5 User defined data block write transaction

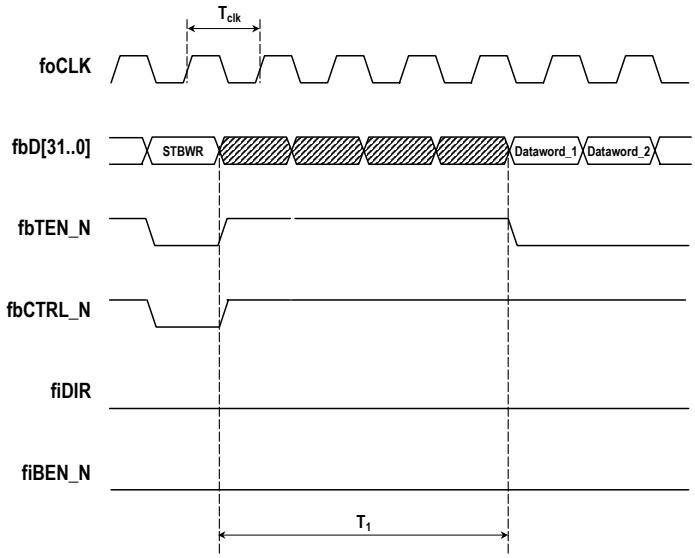


Figure 12 The opening of a data block write transaction

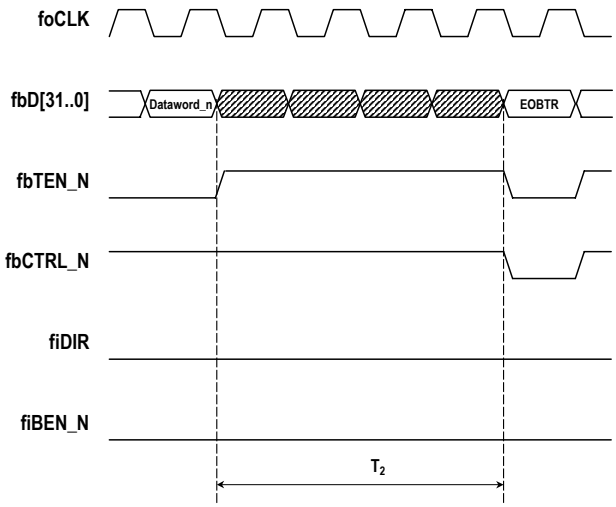


Figure 13 The end of a data block write transaction

Symbol	Parameter	Unit	Min.	Max.
T_{clk}	foCLK clock period	ns	15	-
T_1	the SIU shall transfer the first data word to the FEE after a STBWR command has been transferred from the SIU to the FEE	T_{clk}	4	time-out period
T_2	the SIU shall transfer an EOBRT command to the FEE after the last data word of the data block has been transferred from the SIU to the FEE	T_{clk}	4	time-out period

Table 7 The data block write timing requirements

3.8.6 User defined data block read transaction

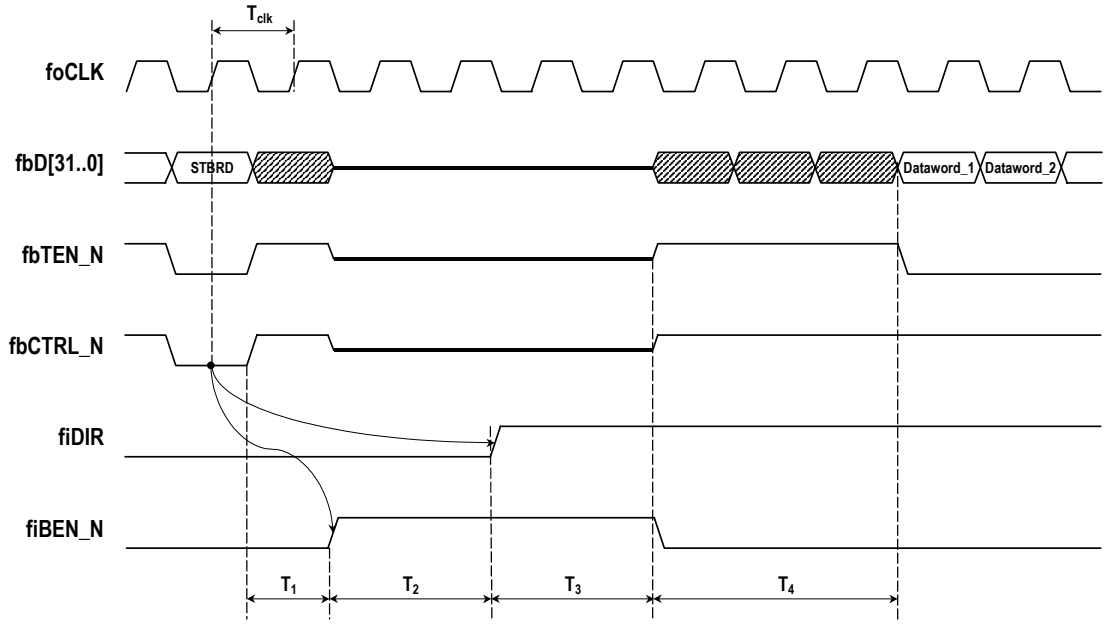


Figure 14 The opening of a new data block read transaction

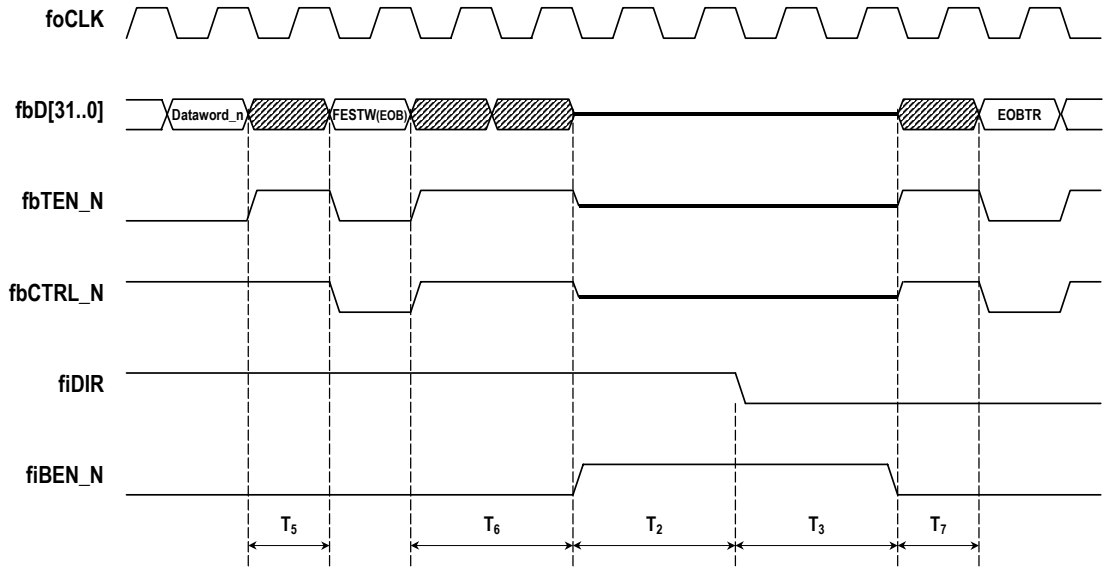


Figure 15 The end of a data block read transaction

Symbol	Parameter	Unit	Min.	Max.
T_{clk}	foCLK clock period	ns	15	-
T_1	the SIU shall put the front-end bus in off-state after a STBRD command has been transferred from the SIU to the FEE	T_{clk}	1	1
T_2	the SIU shall change the direction of the front-end bus after the front-end bus has been put in off-state	T_{clk}	2	2
T_3	the SIU shall put the front-end bus in on-state after the direction of the front-end bus has been changed	T_{clk}	2	2
T_4	the FEE shall transfer the first data word of the data block to the SIU after the front-end bus has been put in on-state	T_{clk}	1	4[11]
T_5	the FEE shall transfer a FESTW with EOB flag=1 to the SIU after the last data word of the data block has been transferred	T_{clk}	0	4[12]
T_6	the SIU shall put the front-end bus in off-state after a EOBTR command has been received by the SIU from the link and the data block transfer from the FEE to the SIU has been finished	T_{clk}	4	4
T_7	the SIU shall transfer an EOBRT command to the FEE after the front-end bus has been put in on-state	T_{clk}	1	1

Table 8 The data block read timing requirements

[11] The front-end time-out bit in the SIU status register will be set to '1', if the FEE do not assert the first data word of the block on the front-end bus within the defined period

[12] The front-end time-out bit in the SIU status register will be set to '1', if the FEE do not assert the FESTW with EOB flag=1 on the front-end bus within the defined period.

3.8.7 Event data transmission transaction

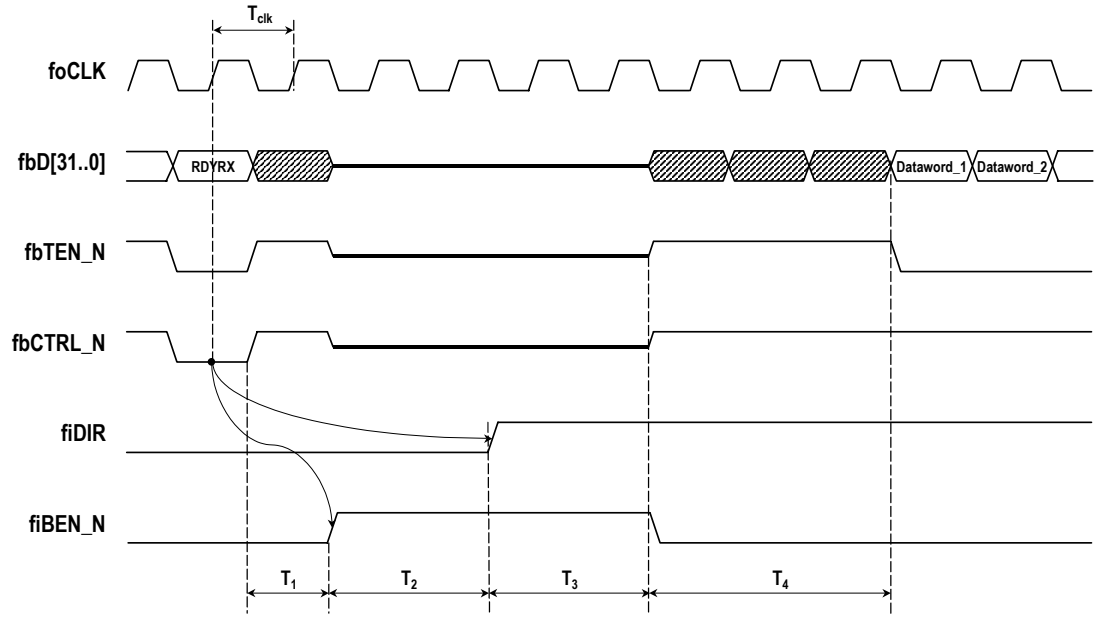


Figure 16 The opening a new event data transmission transaction

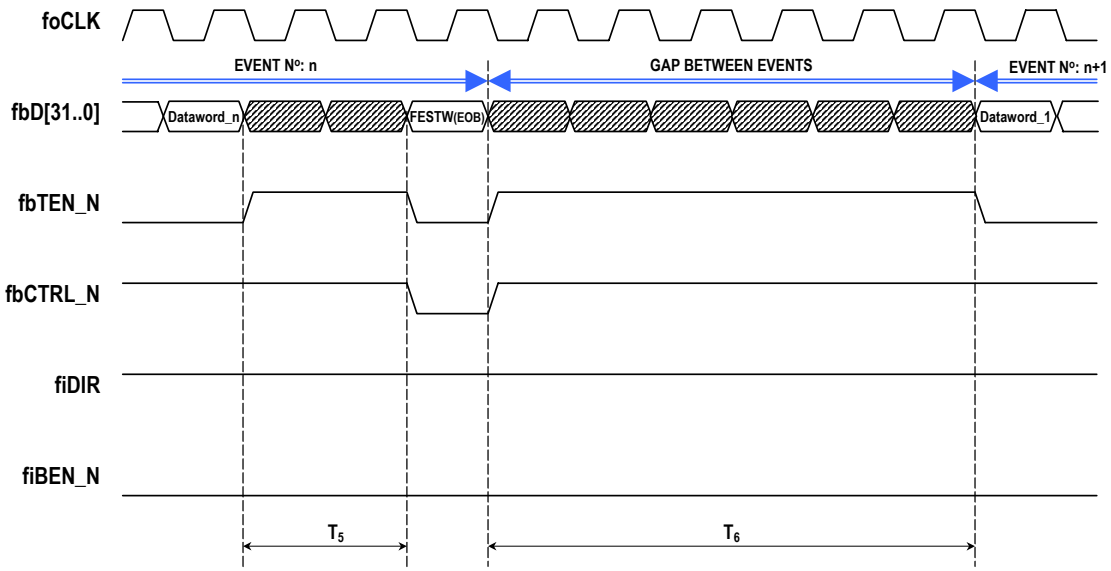


Figure 17 The end of an event transmission and the start of a new event transmission

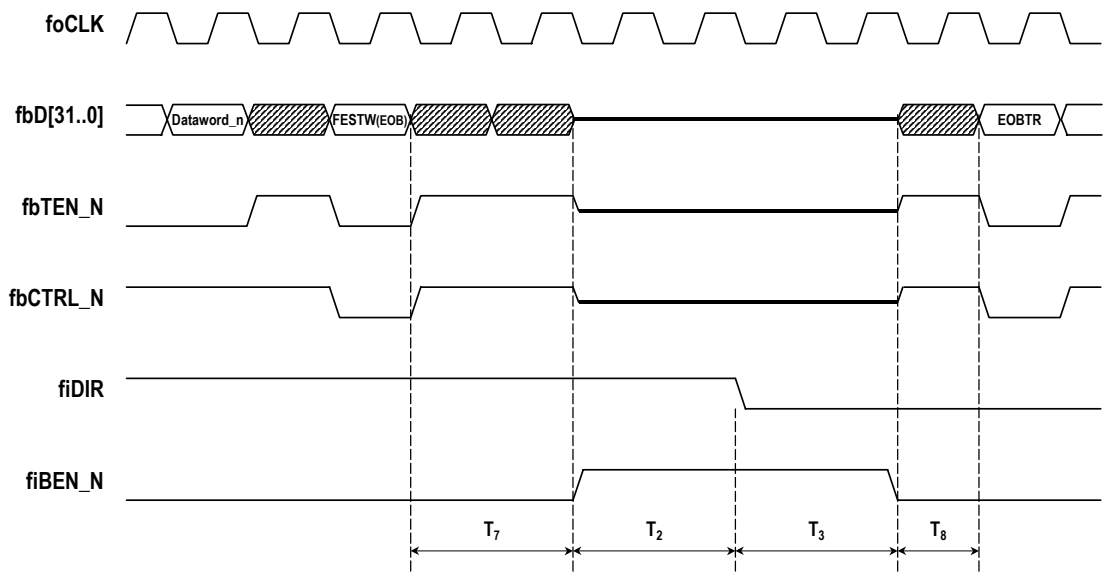


Figure 18 The end of an event data transmission transaction

Symbol	Parameter	Unit	Min.	Max.
T_{clk}	foCLK clock period	ns	15	-
T_1	the SIU shall put the front-end bus in off-state after a RXRDY command has been transferred from the SIU to the FEE	T_{clk}	1	1
T_2	the SIU shall change the direction of the front-end bus after the front-end bus has been put in off-state	T_{clk}	2	2
T_3	the SIU shall put the front-end bus in on-state after the direction of the front-end bus has been changed	T_{clk}	2	2
T_4	the FEE shall transfer the first data word of the first event to the SIU after the front-end bus has been put in on-state	T_{clk}	1	∞
T_5	the FEE shall transfer a FESTW with EOB flag=1 to the SIU after the last data word of the event has been transferred	T_{clk}	0	4[13]
T_6	the FEE shall keep a gap between the transmission of consecutive events	T_{clk}	16	∞
T_7	the SIU shall put the front-end bus in off-state after a EOBTR command has been received by the SIU from the link and an event transfer from the FEE to the SIU has been finished	T_{clk}	4	12
T_8	the SIU shall transfer an EOBRT command to the FEE after the front-end bus has been put in on-state	T_{clk}	1	1

Table 9 The event data transmission timing requirements

[13] The front-end time-out bit in the SIU status register will be set to '1', if the FEE do not assert the FESTW with EOB flag=1 on the front-end bus within the defined period.

3.8.8 Flow control

The SIU shall interrupt the data word transfer to the FEE, when the foBSY_N interface signal is activated by the FEE:

- The SIU shall put the fbTEN_N interface signal to inactive state, when an active foBSY_N signal is sampled by the SIU at the positive edge of the foCLK signal ($\mathbf{t_1}$).
- The SIU shall put the fbTEN_N interface signal to active state, when a inactive foBSY_N signal is sampled by the SIU at the positive edge of the foCLK signal ($\mathbf{t_2}$) and the next data word in the SIU is available for the transfer.

The SIU shall transfer the FECMDs to the FEE, independently of the state of the foBSY_N interface signal. The FEE shall accept the FECMDs, independently of the state of the foBSY_N interface signal. Thus FECMD transfer from the SIU to the FEE shall not be suspended by the flow-control ($\mathbf{t_3}$).

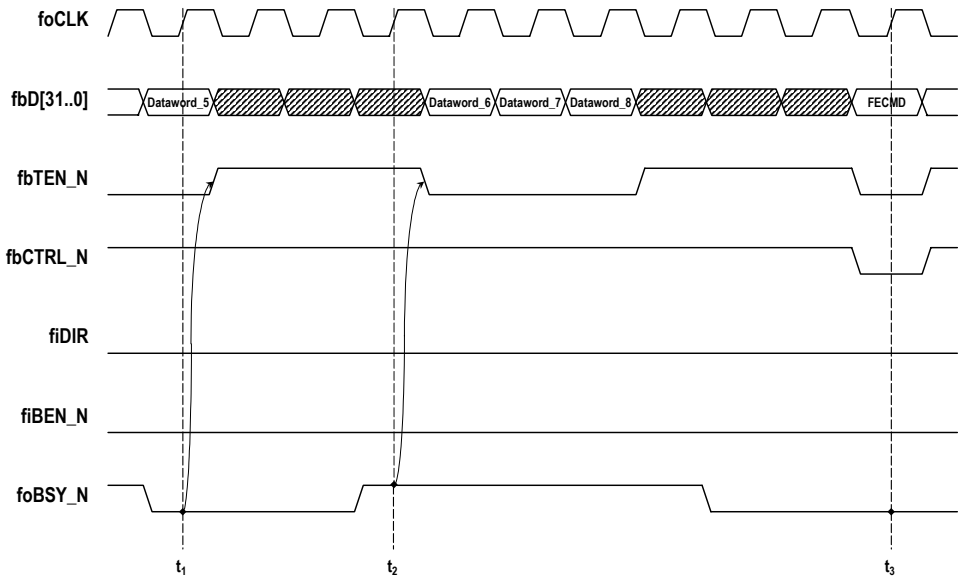


Figure 19 The flow-control for the data transfer from the SIU to the FEE

The FEE shall interrupt the data word transfer to the FEE, when the fiLF_N interface signal is activated by the SIU:

- The FEE shall put the fbTEN_N interface signal to inactive state, when an active fiLF_N signal is sampled by the FEE at the positive edge of the foCLK signal (**t_1**).
- The FEE shall put the fbTEN_N interface signal to active state, when a inactive fiLF_N signal is sampled by the FEE at the positive edge of the foCLK signal (**t_2**) and the next data word is available in the FEE for the transfer.

The FEE shall suspend the transfer of the FESTW(EOB) to the SIU at the end of an event or a data block, when the fiLF_N interface signal is activated by the SIU:

- If the fiLF_N signal is activated by the SIU, the FEE shall not activate the fbTEN_N interface signal, when it is ready to transfer a FESTW(EOB) at the end of an event or a data block (**t_3**)
- Independently of the state of the fiLF_N interface signal, the FEE shall put the fbCTRL_N interface signal to active state, when it is ready to transfer a FESTW(EOB) at the end of an event or a data block (**t_4**).
- The FEE shall put the fbTEN_N interface signal to active state, when a inactive fiLF_N signal is sampled by the FEE at the positive edge of the foCLK signal (**t_5**) and a FESTW(EOB) is available in the FEE for the transfer.

The FEE shall transfer the FESTWs to the SIU, independently of the state of the fiLF_N interface signal. The SIU shall accept the FESTWs, independently of the state of the fiLF_N interface signal. Thus FESTW transfer from the FEE to the SIU shall not be suspended by the flow-control (**t_6**).

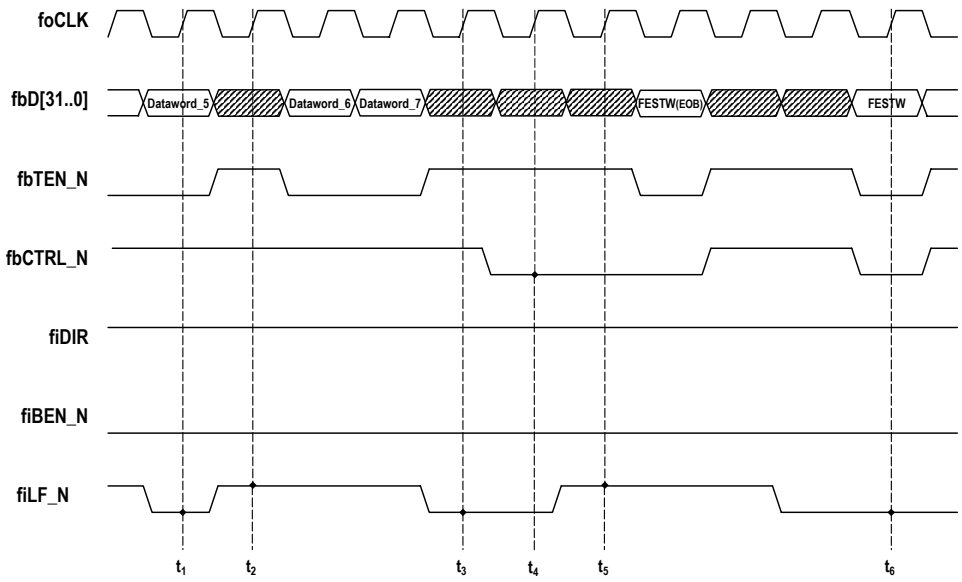


Figure 20 The flow-control for the data and status transfer from the FEE to the SIU

4 Annexes

4.1 Design consideration for FEE motherboard layout

The following rules shall be followed at the design of the FEE motherboard:

- The FEE shall use bus transceivers for the connection of the SIU to the internal front-end bus. Efficient power filtering of the bus transceivers shall be provided. The *IDT 74LVCHR162245A* is the suggested bus transceiver family.
- The maximum length of the routed lines from the SIU connector to the bus transceiver chips is strictly limited to 40 mm. Terminations on the SIU-FEE interface lines are not required (the line length is limited to avoid transmission line effects).
- Solid GND plane in the board stack-up shall be used under the lines from the bus transceivers to the SIU connector.
- Placing components on the FEE motherboard under the SIU card is limited by space and by height. The envelope is specified by the CMC specifications.
- The +3.3 V pins of the SIU connector shall be connected directly to the internal and +3.3 V power planes of the FEE mother board or they shall be connected to the power lines by a low impedance connections.
- The signals of the TAP shall be connected to different bus transceivers than the FEE-SIU interface signals.

JTAG interface description (preliminary)

The aim of this document is to provide information for the front-end designers about the DDL-JTAG interface. The JTAG port is part of the SIU-FEE interface and consists of the standard JTAG signals, i.e. TCK, TDI, TDO, TMS and TRST (see Table 4). This JTAG interface can be used to download parameters to the front-end electronics or collect status information of the electronic components.

The idea is to have a virtual JTAG channel that operates together with the data transfer. At the front-end side the JTAG signals are implemented. The DDL control software shall offer the API to control these signals so that the whole DDL can act like an expanded JTAG port. The operation shall be completely transparent to the user.

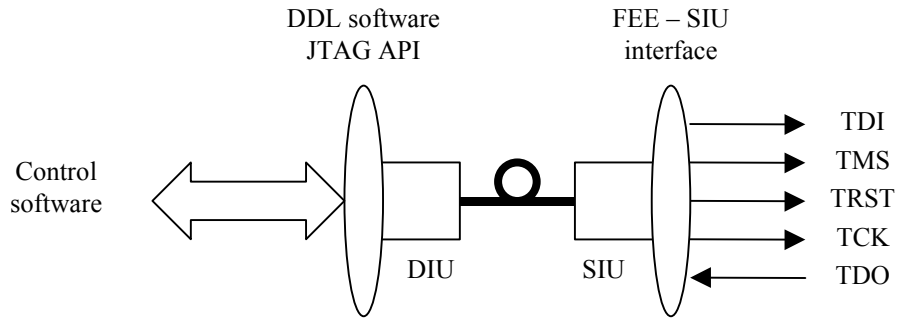


Figure 21 Basic structure of the JTAG chain.

The usage of this interface is very simple. The front-end designer shall connect the JTAG port signals to the chain built on the FEE. The port shall provide serial data transfer at different transfer rates. The required rate can be set by the control software.

Since this implementation is a simple JTAG expander it is the user responsibility to prepare the bit sequence that should be transferred through the chain. This means that the control software shall give the required value of the TDI, TMS and TRST signals for each TCK period packed in a 32-bit word. The bit mapping of the 8 JTAG periods (from bit period N to period N+7) is shown in Table 10.

31	30	29	28	27 – 8	7	6	5	4	3	2	1	0
Reserved	TRST(N+7)	TMS(N+7)	TDI(N+7)	…	Reserved	TRST(N+1)	TMS(N+1)	TDI(N+1)	Reserved	TRST(N)	TMS(N)	TDI(N)

Table 10 Mapping of the TDI, TMS and TRST signals

During the transfer the captured TDO signal shall be packed in a 32-bit word and sent back via the DDL. In order to save the bandwidth of the backward channel (from the FEE to the RORC) one word shall contain 32 bits of the TDO signal, i.e. each bit corresponds to one TCK period.

An example of the operation can be seen in Figure 22. The consecutive bit periods are unpacked from the input word and the TCK signal is generated at the required frequency. The TDO signal is sampled and stored in the output word.

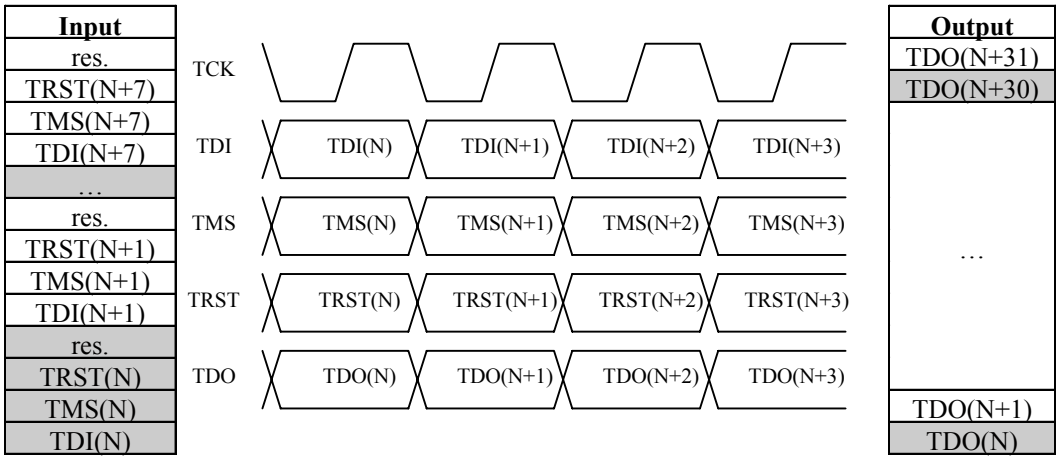


Figure 22 Example of the JTAG operation

5 Notes